A Laboratory Course in
ELECTRONICS

Ramalingom & Raghupalan

59-0

২৫৭

A Laboratory Course in
ELECTRONICS

A LABORATORY COURSE IN ELECTRONICS

T. RAMALINGOM
University Service and Instrument Centre,
Madurai Kamaraj University, Madurai

P. RAGHUPALAN
Electronics Fabrication Facility,
Vikram Sarabhai Space Centre, Trivandrum

2259

OXFORD & IBH PUBLISHING CO.
New Delhi Bombay Calcutta

© 1980, T. Ramalingom, P. Raghupalan
Second Printing 1985

ISBN 81-204-0057-7

Published by Mohan Primlani for Oxford & IBH Publishing Co.,
66 Janpath, New Delhi 110001 and printed at
Chaman Offset Printers, Suiwalan, Darya Ganj, Delhi 110002

Accno-16411

FOREWORD

Engineering practice is based on the application of one or more of the following tools:

(i) Mathematical analysis
(ii) Laboratory or field experiments
(iii) Engineering judgement

Experimentation and the use of inductive reasoning provide the most important means of understanding nature and finding truth. Experimentation helps not merely in verification, but also in gaining new insight and understanding. Laboratory practice in an educational institution must aim at educating and training the student in the effective use of the experimental method in solving problems.

In the recent years, reasonably good textbooks, that deal with analysis and design in Engineering and Technology, have been published. Good books on Laboratory practice are the desideratum. Viewed from this angle, this book on *Laboratory Course in Electronics* is a welcome addition and a valuable contribution.

The authors are instrument/electronic engineers and are associated with such major institutions of learning/research as the Central Instrumentation Laboratory, Madurai Kamaraj University; and the Vikram Sarabhai Space Centre. They are well prepared, in terms of their theoretical preparation and practical experience, for undertaking a job of this nature.

The book attempts at giving a comprehensive Laboratory Course on Electronics. It contains fifty-four kinds of circuits, chosen carefully on the basis of their practical and professional importance. Besides giving a procedure for conducting experiments, the students are given some insight into the basic principles and design considerations for furthering their knowledge through deeper studies. The book also deals with various kinds of instruments used in electronics laboratories.

It is my considered opinion that this book is a valuable addition to the literature on laboratory practice and will be quite useful for both the teachers and the students in academic institutions.

Director of Technical
Education, Tamil Nadu
(On deputation to the UNESCO,
Colombo)

Dr. V.C. KULANDAISWAMY

PREFACE

This book has been written to satisfy the needs of engineering colleges, polytechnics and other technical institutions which are offering courses in electronics and electrical engineering. This is an attempt to give comprehensive knowledge to the students on laboratory course in electronics. This book contains carefully chosen 54 different kinds of circuits of high practical and professional importance. The practical approach devoid of theory misses the point by failing to satisfy the basic human curiosity. So, besides giving a procedure for conducting experiments, the students are given some insight into the basic principles and design consideration for furthering the knowledge through deeper studies. A separate part on various kinds of test and measuring equipments used in the electronics laboratory is also dealt with. The authors are highly indebted to Dr. V. C. Kulandaiswamy, Director of Technical Education, Tamil Nadu (on deputation to the UNESCO, Sri Lanka) for his Foreword on this book.

The cordiality and thoughtful suggestions of the staff of Oxford & IBH Publishing Company are gratefully acknowledged.

T. Ramalingom
P. Raghupalan

CONTENTS

Foreword v
Preface vii

PART I
EXPERIMENTS 1

1. Passive Differentiator Circuit 3
2. Passive Integrator Circuit 6
3. Time Constant Circuit 8
4. Diode Characteristics 11
5. Rectifier Circuit 15
6. Zener Diode Characteristics 19
7. Transistor Characteristics 22
8. Leakage Current of Transistor 25
9. Transistor Biasing 28
10. Bias Point Stability of a Transistor under DC Conditions 32
11. Small Signal Common-Emitter Transistor Amplifier 36
12. Emitter Follower 40
13. Direct Coupled Amplifier 43
14. Transformer Coupling in Amplifiers 46
15. Tuned Amplifier 51
16. High Input Impedance Transistor Amplifier 54
17. Differential Amplifier 56
18. Negative Feedback Amplifier 60
19. Transistor Amplifier—Signal Limitations 64
20. Forward Current Transfer Ratio of a Transistor 67
21. Low Frequency Response of a Transistor Amplifier 70
22. High Frequency Response of a Transistor Amplifier 73

23. Transformer Coupled Power Amplifier 76
24. Push-Pull Transformerless Class B Power Amplifier 79
25. Operational Amplifier 82
26. Operational Amplifier—As Summing Amplifier 86
27. Phase Shift RC Oscillator 88
28. Colpitts Oscillator 92
29. Crystal Oscillator 95
30. Bistable Multivibrator 97
31. Schmitt Trigger 101
32. Collector Coupled Monostable Multivibrator 104
33. Emitter Coupled Monostable Multivibrator 109
34. Astable Multivibrator Collector-Coupled 114
35. Pulse Transformer 119
36. Blocking Oscillator 123
37. Synchronisation Technique in Astable Multivibrator 127
38. Characteristics of a Series Regulator 129
39. Silicon Controlled Rectifiers 133
40. DC to AC Invertor 139
41. Ramp Generator 142
42. Diode Clippers 144
43. Diode Clampers 147
44. Transistor Switching 150
45. Diode Resistor Logic Circuits 153
46. Transistor Logic Circuits 157
47. Linear Sweep Circuit 161
48. Unijunction Transistor 164
49. Field Effect Transistor 168
50. Tunnel Diode Characteristics 172
51. IC Regulator 174
52. IC Comparator 179
53. IC Timer Circuit 182
54. TTL Gates 185

PART II
EQUIPMENTS

55. Multimeter 193
56. Vacuum Tube Voltmeter 195
57. Transistor Voltmeter 200
206

58. Transistor Tester 208
59. Universal Impedance Bridge 211
60. Signal Generator 213
61. Cathode Ray Oscillator 215
62. Digital Frequency Counter 226
63. Digital Voltmeter 230
64. Power Supply 234
References 237
Appendix 238

1

PASSIVE DIFFERENTIATOR CIRCUIT

Theory

A very short time constant RC or RL circuit works as a differentiator. Such a circuit differentiates the input square wave into pulses. Differentiators are frequently referred to as high pass filters. The word differentiation refers to rate of change, slope of curves, speed, acceleration, etc. The process of differentiating an equation results in another equation called the derivative. In an RC differentiator circuit the voltage across the resistor, e_R can be seen on a CRO. Differentiation accuracy improves with shorter time constant through the reduction of resistance in RC circuit, to the minimum practical values. Similarly in a short time constant RL circuit waveform across the inductor gives the derivative of mathematical expression for the current in the circuit. Rectangular waveforms are converted into spike voltages which are used as triggers for other wave shaping circuits. For non-rectangular waveforms, the differentiator generates different shaped waveforms.

From the charge equation of capacitance we know that $Q = CV$ where V is the voltage across the capacitor C. For a small change in Q, we can write the equation as $\Delta Q = C\Delta V_C$. If we divide both sides by Δt, the time interval in which these small changes take place, we get the expression: $\Delta Q/\Delta t = C. \Delta V_C/\Delta t$.

Expression for current is Qt. That is $i = C.\Delta V_C/\Delta t$. Voltage across the resistor $R = RC\, \Delta V_C/\Delta t$. Since $RC = T$,

Voltage across the resistor $e_R = T.\Delta_C/\Delta t$.

Thus the differentiator voltage is the product of circuit time

constant and rate of change of capacitor voltage. Similarly for *RL* circuit of short time constant, the differentiation action comes across the inductor. Writing the voltage equation for inductor, we get $e_L = L.di/dt$ but $i = dQ/dt$.
Therefore di/dt is a derivative of $\Delta Q/\Delta t$.

If the current is the rate of change of movement, then, di/dt is the acceleration of the movement. The instantaneous voltage across the inductor e_L is dependent on the rate at which the current is changing. Dividing the equation $e_L = L.di/dt$ by R, we get $e_L = T.R.\ di/dt$ where $T = L/R$. Thus we find the differentiator voltage is the product of circuit time constant, resistance and the rate of change of current. Thus *RC* circuit differentiates the voltage across the capacitor and *RL* circuit differentiates the current through the inductor.

Objective

To study *RC* differentiator circuit.

Experimental Set Up

Equipments needed

1. Square wave generator—1 No.
2. Oscilloscope—1 No.

Components required

1. Capacitance of suitable value (0.1 mfd)—1 No.
2. Resistance of suitable value (1 kilo ohm)—1 No.

Procedure

Rig up the circuit as shown in the Fig. 1.1. Feed from the square wave generator positive going voltage of amplitude, say, 5 volts peak to peak to the circuit. Observe the waveform across the resistor on an oscilloscope. The positive going wave produces

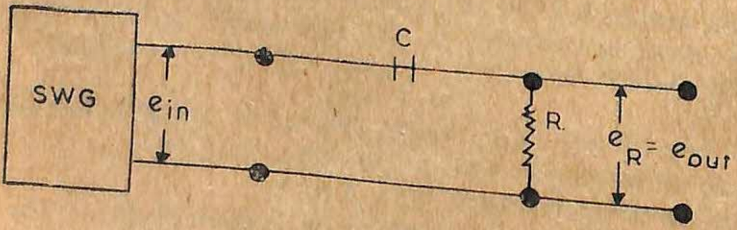


Fig. 1.1

positive and negative going pulses of equal amplitude. Observe the shape of the pulses. Vary the *PRF* of the input signal and observe the shape of the pulses. Find out the optimum *PRF* of the generator to obtain well-differentiated pulses. For different values of *R* and *C* repeat the experiment.

Review Questions

1. Study the impact of a higher *PRF* on the shape of the pulses and give the reasons.
2. What is the effect of leakage resistor across the capacitor on the wave shape at the output?

2

PASSIVÈ INTEGRATOR CIRCUIT

Theory

Integrator circuits are known as long time constant circuits. They are sometimes referred to as low pass filters. Integrator circuits perform the summing up action. In an *RC* circuit, the voltage across the capacitor gives the integrating action and the voltage developed across the resistor in the *RL* circuit gives the same phenomenon. Writing the current equation in the capacitor we get, $i_C = \Delta Q/\Delta t$. That is $\Delta Q = i_C \Delta t$. But the voltage across the capacitor $v_C = Q/C$. An addition of a small charge, Q, results in a change of voltage v_C in the capacitor.

That is, $\Delta v_C = \Delta Q/C$. That is, the capacitor voltage rises with every increase in the charge. Mathematically putting, $v_C = I/C \int i_C dt$.

That is, the v_C is the measure of the sum of all charges stored in the capacitor.

For the *RL* integrator circuit, voltage across the resistor R, $v_R = i_L/R$ at any moment. For a small change in current, the change in voltage $\Delta v_R = \Delta i \times R$. The rate of change of current for a short duration can be written as $\Delta i/\Delta t$. This can be equated as $di/dt = v_L/L$. The current at any instant will be the sum of all the small current changes. Therefore, the instantaneous voltage across the resistor $v_R = 1/T \int v_C . dt$. That is the voltage drop v_R is the measure of current changes as a result of induced voltage v_L.

Objective

To study the integrator *RC* circuit.

Experimentel Set Up

Equipments needed

1. Function generator—1 No.
2. Oscilloscope—1 No.

Components required

1. Capacitor of suitable value (0.1 mfd)—1 No.
2. Resistor of suitable value (10 kilo ohms)—1 No.

Procedure

Make the corrections as per the details shown in Fig. 2.1. Feed a square wave of amplitude, say, 5 V_{pp} and observe the waveform across the capacitor. Vary the *PRF* of the function generator and see the wave shape. Note down the *PRF* at which the output waveform is as good a triangular waveform as possible. Repeat the experiment for different values of *R* and *C* and note the *PRF* for different time constants.

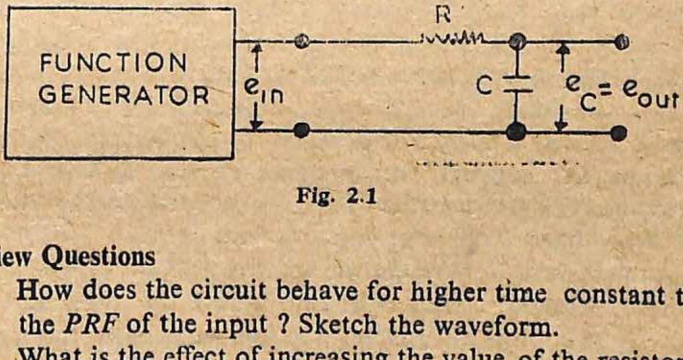


Fig. 2.1

Review Questions

1. How does the circuit behave for higher time constant than the *PRF* of the input ? Sketch the waveform.
2. What is the effect of increasing the value of the resistor for a same time constant from that of a previous value ? How does the amplitude of the waveform change ?

3

TIME CONSTANT CIRCUIT

Theory

Electrical behaviour of resistance, capacitance and inductance, accounts for the wave shaping properties of linear circuits. They are generally of series connected *RC*, *RL* and *RLC* combinations. The shape of purely sinusoidal waveforms is not altered by linear wave shaping circuits though amplitude and phase relationships are modified. But waveforms like rectangular, square, sawtooth, etc., are modified by such circuits. The extent of such alterations depend upon time-constant (*T*) and the shape of applied signals. For example, a step voltage applied to the series *RC* network will produce initially a large current because of the characteristics of the capacitor to lead the current over the voltage. This large initial current causes a voltage drop across the resistor in the opposite polarity. As the charge in the capacitor increases, the counter emf across the capacitor also rises. If the level of the applied step voltage persists, the rate at which the capacitor continues to charge reduces with time. The applied voltage is countered by capacitor voltage.

Objective

To study *RC* and *RL* series circuits characteristics.

Experimental Set Up

Equipments needed

1. Square wave generator—1 No.
2. Oscilloscope—1 No.
3. Impedance bridge—1 No.

Components required

1. Suitable values of resistor, capacitor and inductance.
2. Resistor 100 ohms, 1 kilo ohms, 10 kilo ohms and 100 kilo ohms.
3. Capacitor 0.01 mfd, of low leakage resistance type.
4. Inductor 30 mh (*RF* choke).

Procedure

Measure the values of R, L and C using an impedance bridge and record their values. Measure the dc resistance of the inductor. Compare the values of time constants for RC and RL circuit combinations. Time constant $T = RC$ or $L/R+R_{dc}$. After making the connections as shown in Fig. 3.1, feed a signal from a square wave signal generator at a constant amplitude of, say, $2V_{pp}$ and observe the voltage waveform across the capacitor in the oscilloscope. From the observed waveform calculate T (time taken for charging the capacitor to 62.3% of the maximum value). Compare this against the theoretical value calculated above. Vary the *PRF* in the square wave generator and note the time constants as explained above. Repeat the experiment for different time constants by varying the resistance.

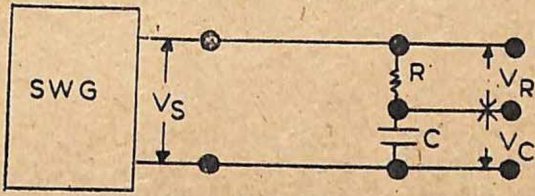


Fig. 3.1

Rig up the circuit as shown in Fig. 3.2. Observe the waveform across the inductor in the oscilloscope and compute the time

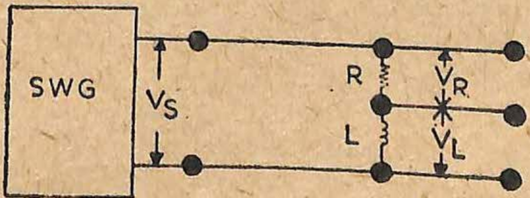


Fig. 3.2

constants as explained in the above paragraph. Repeat the experiment as in the case of *RC* circuit.

Review Questions

1. Find out the optimum *PRF* for a waveform across the capacitor.
2. Increase the *PRF* over the optimum value and observe the waveform. Explain the reasons for the distortion in the waveform.

4

DIODE CHARACTERISTICS

Theory

Junction diodes biased in the forward direction exhibit relatively low resistance, *E/I* equals a few ohms. Diodes biased in the reversed direction exhibit high resistance. *E/I* equals hundreds of kilo ohms or even mega ohms depending upon the material used for the construction of the diode and the construction method. That is, the diode works as a switch *on* in the forward direction and *off* in the reverse direction. Important consideration is whether the majority or minority carriers produce the current across the diode *p-n* junction. The junction is manufactured with *p* and *n* materials having predominantly majority carriers. Still there are a few minority carriers also present in the junction. This minority carriers account for small currents in the reverse biased condition. Forward bias produces large majority carrier currents. Thus forward bias can be considered as closed or on switch. Reverse bias can be regarded as an open switch.

At high switching speeds, capacitance effect becomes very important in semiconductor diodes. This results in 'miller effect'. The unbiased diodes will have a net charge of zero on both sides of the *p-n* junction. Application of forward bias causes drift of carriers across the junction. The rate of carrier charge flow is proportional to the potential applied across the diode. The characteristic of an ideal diode is shown in Fig. 4.1 (a). This curve shows the ideal characteristics. The practical diode characteristics is as shown in Fig. 4.1 (b).

In Fig. 4.1 (b), the forward current starts increasing in a non-

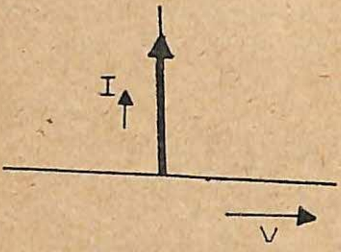


Fig. 4.1 (a)

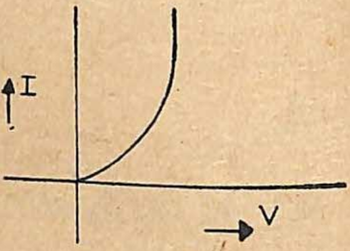


Fig. 4.1 (b)

linear fashion and the rate of increase is negligible till a small voltage. This voltage is called the 'barrier potential'. This means that the diode starts conducting only if the potential applied is beyond the barrier potential. The rate of increase of current is very high when the input voltage exceeds this barrier potential.

Objective

To become familiar with diode characteristics.

Experimental Set Up

Equipments needed

1. VTVM—1 No.
2. Multimeter—1 No.
3. Variable DC source —1 No.

Components required

1. Protection resistor—1 No.
2. Diode—1 No.

Procedure

Choose a typical diode for the experiment. From the data sheet, note down the rated current and the maximum reverse voltage applicable for the diode. Draw the circuit as shown in Fig. 4.2 and label all the parts. The resistor R is chosen to limit the maximum current in the diode. $R = E_{\max}/I_{\max}$. Choose appropriate current range in the multimeter for forward current measurements. Vary the source voltage in suitable steps and measure the forward current. Record the measurements and calculate the value of forward resistance from the graph.

Before making reverse biased measurements, the circuit is modified as shown in Fig. 4.3. Choose appropriate current range

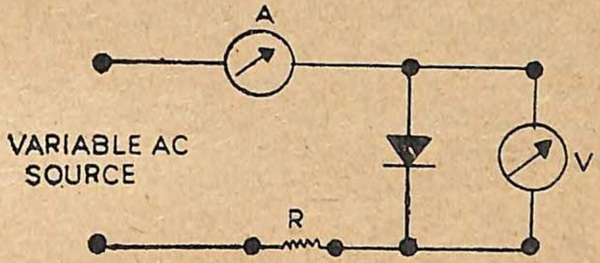


Fig. 4.2

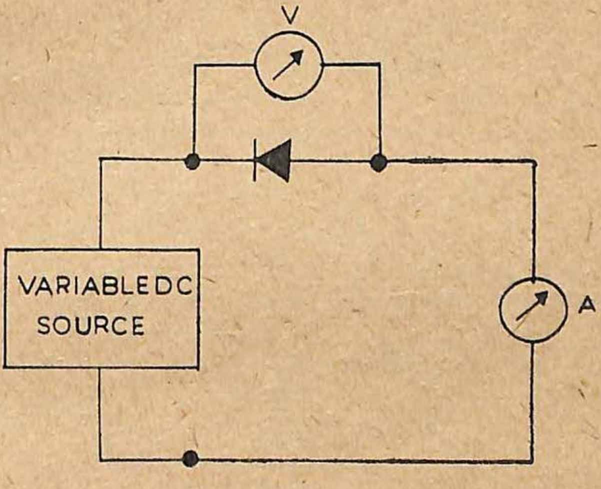


Fig. 4.3

in the multimeter for reverse current measurements. At least make six measurements between zero and reverse breakdown voltage and record the same. Construct a graph of current versus voltage. Use ordinate as current scales such that one scale unit for forward biased current has ten times the value of the reverse biased current. Plot abscissa voltages, using scales such that one unit reverse bias has ten times the value of the forward bias.

Review Questions

1. Graphically determine the incremental forward conductance for different currents.

2. What is the approximate turn-on valtage for germanium and silicon diodes ? What are the reasons for these values being different ?
3. What are the reasons for higher reverse currents in a diode ?
4. Is the conductance of a diode in the forward biased condition dependent on forward current ?

5

RECTIFIER CIRCUIT

Theory

The active circuits of electronic equipments operate on dc voltages. These voltages are derived from the conventional ac line voltages using power rectifiers of suitable ratings. Power supply performance has got a direct bearing on the quality of any equipment. Therefore, it is necessary to understand the different types of rectifications possible to provide good dc potentials. Broadly the rectifiers can be classified into (*i*) half wave rectifier, (*ii*) full wave rectifier with central tap and (*iii*) bridge rectifier. Half wave rectifier shown in Fig. 5.1 conducts for only one half of the supply voltage and discharges during the other half of the waveform. Because of this, there is a great deal of ripple voltage in the output and hence stability is poor.

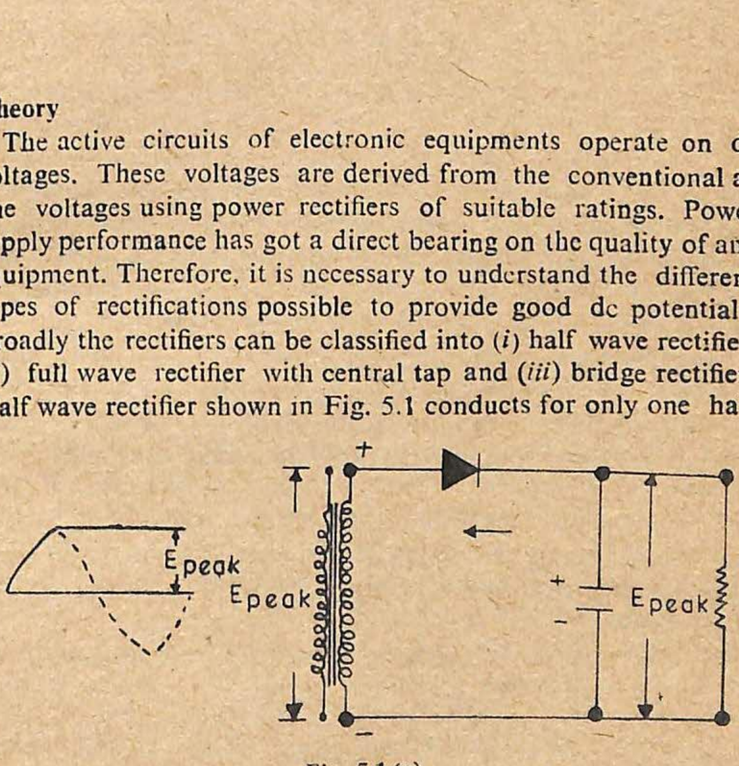


Fig. 5.1 (a)

From Fig. 5.1 (b), it is obvious that the condenser starts discharging from the moment the supply voltage starts falling from the peak. This continues till time T_2 when the supply voltage goes towards positive peak. During the period T_2 to T_3, the con-

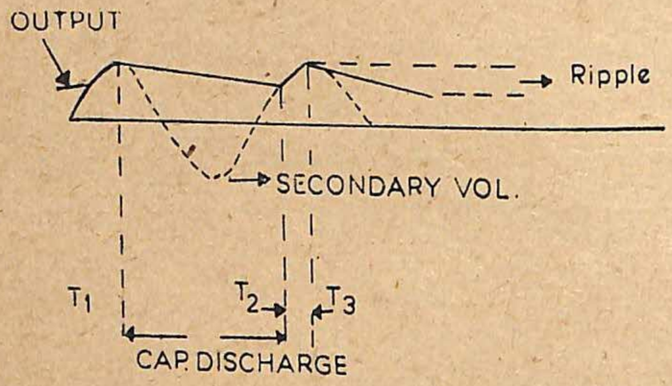


Fig. 5.1 (b)

denser gets charged upto the peak value. During the negative half of the cycle, peak inverse voltage developed across the diode is twice the peak supply voltage. In order to use a diode as a half wave rectifier the minimum reverse voltage capability of the diode should be twice the peak supply voltage.

The full wave rectifier shown in Fig. 5.2 is an improvement over the half wave rectifier. Here both the half cycles are rectified by the diodes D_1 and D_2 and the ripple voltage is reduced to a minimum. The peak inverse voltage of the individual diode is only half that of the half wave rectifier. In this type of rectifiers, secondary transformer has to be wound for twice the voltage with a centre tap. Hence one more winding in the transformer is required. This is amply rewarded in terms of improved performance.

Another version of rectification using a single winding in the secondary transformer is possible by using a bridge rectifier. Here four diodes are connected in the form of a bridge as shown in Fig. 5.3. The current directions are shown with the arrow marks. When the potential ab is positive, the diode D_1 conducts charging C_1 completing the circuit through the diode D_4. During the other half of the cycle, conduction takes place through the diode D_2, C_1 and D_3. The advantages of full wave rectifier over half wave rectifier is that the former has low ripple content over the latter. The ripple frequency of the full wave rectifier is twice the line frequency whereas that of half wave rectifier is same as the line frequency.

Objective

To study the characteristics of rectifier circuits.

Experimental Set Up

Equipments needed

1. Multimeter—1 No.
2. Transformer with a centre tap secondary of suitable current rating—1 No.
3. Oscilloscope—1 No.
4. Rheostat—1 No.

Components required

1. Diodes—4 Nos.
2. Condenser of suitable voltage rating—1 No.

Procedure

Wire the circuits as shown in Figs. 5.1-5.3 one after the other. Give the power connections and note the dc output voltage using a multimeter. Using an oscilloscope, find out the ripple voltage. Vary the load and repeat the above observations and note the difference in the ripple content and output voltage for various load currents. Change the value of the condenser and repeat the experiment to study the performance of the rectifier.

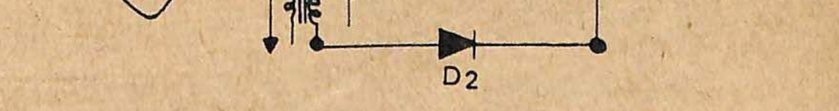


Fig. 5.2 (a)

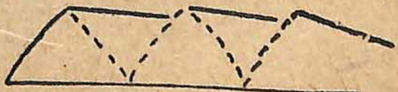


Fig. 5.2 (b)

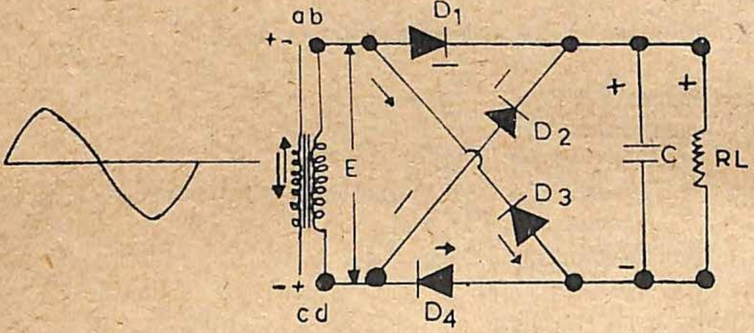


Fig. 5.3 (a)

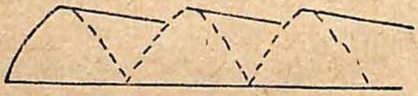


Fig. 5.3 (b)

Review Questions

1. Compare the theoretical average value of the half wave rectifier output and compare the same with the observed value.
2. Why should the *PIV* of a half wave rectifier diode be twice that of the supply voltage ?
3. What is the theoretical average value of the output voltage for the full wave rectifier and compare the same with the observed values ?
4. Discuss the advantage of the bridge type rectifier over a full wave rectifier circuit.

6

ZENER DIODE CHARACTERISTICS

Theory

Zener diode is designed primarily for operation in the breakdown region. It is by this parameter that zener diodes of a given family of 'typed' and likewise breakdown voltage becomes a very important design parameter when used in circuit applications. A reverse voltage applied across the diode with necessary protective resistor causes the diode to enter the breakdown or high reverse current region. The specification sheets of the zener diodes refer this breakdown voltage as V_z or E_z.

Referring to Fig. 6.1, it would be easy to note V_z as the voltage at the exact point of transition. For several low voltage zener diodes as shown in Fig. 6.2, sharpness is not very much evident. For curves 1 and 2 in the figure it would be hard to say just where the knee really is. Zener diodes are available with break-

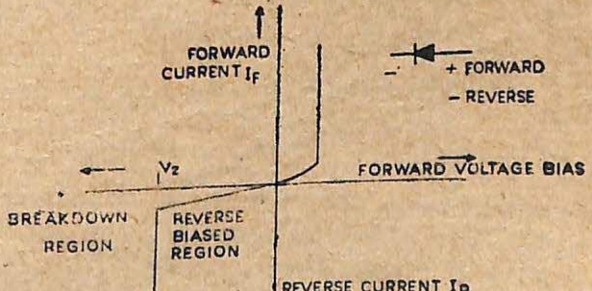


Fig. 6.1

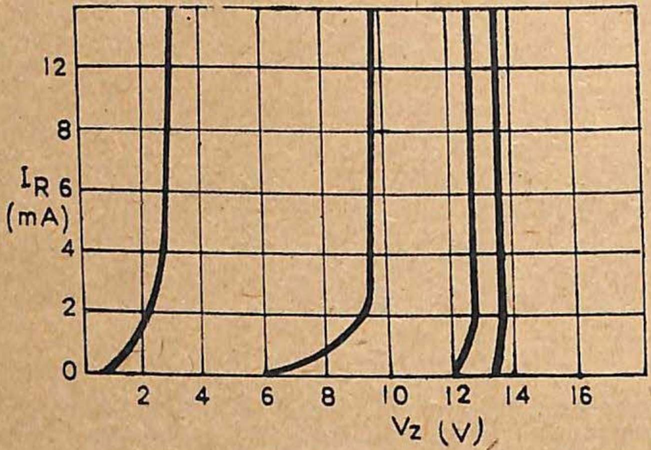


Fig. 6.2

down voltages from 2.42 to 200 volts. Normally low voltage diodes with V_z below 6.2 volts are made by alloy junction process and those having V_z of 6.8 volts or higher are usually made by diffusion process. The resistivity of the material used in making different breakdown voltage zener diodes is different. We may expect some substantial variation in the breakdown characteristics as is evident from the curves shown in Fig. 6.2. The breakdown voltage of a zener diode will vary with temperature. The temperature coefficient of zener breakdown is negative for low voltage below 6.0 volts and positive for higher voltages.

Objective

To find the breakdown voltage and effective resistance of the zener diode.

Experimental Set Up

Equipments needed

1. VTVM or Multimeter—1 No.
2. Variable dc source—1 No.
3. Ammeter—1 No.

Components required

1. Protection resistor—1 No.
2. Zener diode—1 No.

Procedure

Find out from the data sheet the typical breakdown voltage of the zener diode. Let it be V_z. Let the variable source voltage be V_B. The value of V_B should be greater than V_z. Find out the minimum zener current for breakdown, $I_{z\,\min}$. Then calculate $R_{\max}$ equal to $\frac{V_B - V_z}{I_{z\,\min}}$. Vary the input voltage from zero and measure the values of V_z and I_z from the meters. Continue this till the voltage shown in the meter corresponds to typical breakdown voltage. Note the values of I_z. Vary the input voltage further such that I_z does not exceed the maximum rated value and note down the values of V_z and I_z. Immediately turn off the voltage to a lower level to protect the zener from damage. Draw a curve with variable input voltage as abscissa and the zener current as ordinate. From the graph calculate the breakdown and effective resistance of the zener diode as explained in Fig. 6.4.

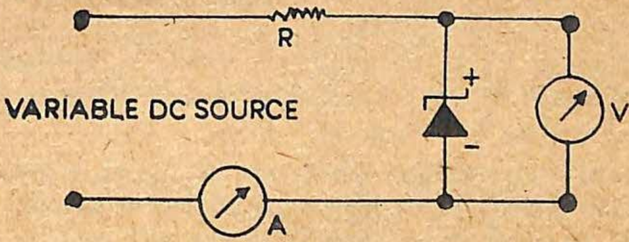


Fig. 6.3

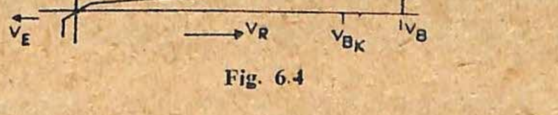


Fig. 6.4

Review Questions

1. How does the zener action take place ?
2. What is the reason for the temperature coefficient of the diode to spread over positive and negative regions ?
3. How does dynamic resistance in a zener diode behave in the breakdown region with current ?

7

TRANSISTOR CHARACTERISTICS

Theory

The static characteristic curves of the transistor define the steady-state relationships among its input, output currents and voltages. These curves are obtained through DC measurements. These characteristics enable graphical design procedures and description of transistor performance under nonlinear conditions. The characteristic curves constitute the basis for understanding the transistor operation. The transistor, a 3-terminal device, has six variables comprised of three currents and three voltages as shown in Fig. 7.1. Since any two currents or any two voltages determine the third respective quantity, the actual number of variables reduced to four. Thus with the knowledge of any two of the variables, the others can be determined.

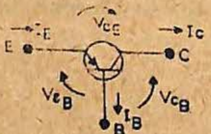


Fig. 7.1

Objective

To determine the common-base and common-emitter characteristics of a transistor.

Experimental Set Up

Equipments needed

1. One variable power supply 30V/1A—1 No.
2. One variable power supply 5V/1A—1 No.
3. Ammeter 0-100 ma—1 No.
4. Ammeter 0-1 ma—1 No.
5. Voltmeter 0-30V—1 No.

Components needed

1. Test transistor (low power) of suitable voltage and current ratings.
2. Resistors—2 Nos.

Procedure :

Give connections as shown in Fig. 7.2 for common-base configuration. Choose a carbon film resistor of value 100 ohms,

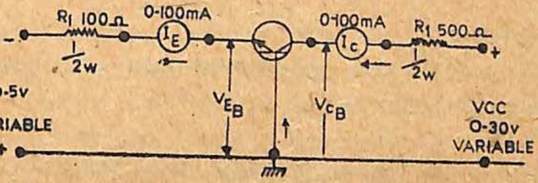


Fig. 7.2

½ *W* for R_1 and a carbon film resistor of value 500 ohms, ½ *W* for R_2 to limit the current excursions in the circuit. Vary V_{EE} so that I_E is arround 2 ma. Adjust V_{CC} to get V_{CB} as zero. Note the value of V_{EB}. Keeping V_{CB} as zero volt, vary I_E by varying V_{EE} and note the values of V_{EB} and I_E. Repeat the experiment with V_{CB} as one volt for I_E in steps of 2 ma. Draw a graph connecting I_E and V_{EB} for different values of V_{CB}. Adjust V_{EE} so that I_E is zero. Vary V_{CC} and note V_{CB} and I_C. Vary V_{EE} so that I_E is about 2 ma. Vary V_{CC} from zero to a suitable value and note the values of V_{CB} and I_C. Repeat the experiment for I_E in steps of 2 ma. Draw a graph connecting V_{CB} and I_C for different values of I_E.

Give connections as shown in Fig. 7.3 for common-emittor configuration. Choose a carbon film resistor of value one kilo ohm, ½ *W* for R_1 and a carbon film resistor of value two kilo ohms. ½ *W* for R_2 to limit the current excursions in the circuit. Adjust the value of V_{CC} so that V_{CE} is zero. Vary V_{BB} and note V_{BE} for different values of I_B. Repeat the above experiment for V_{CE} is equal to one volt. Draw a graph connecting I_B and

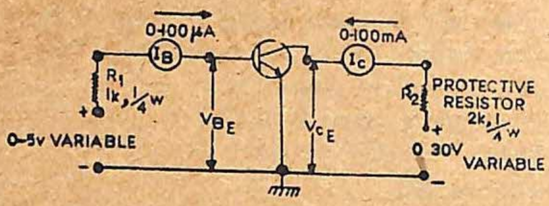


Fig. 7.3

V_{BE} for different value of V_{CE}. Vary V_{BB} so that I_B is, say, 10 micro amperes. Vary V_{CE} in steps of 5 volts and note V_{CE} and I_C. Repeat the experiment for different values of I_B in steps of 10 micro amperes. Draw a graph connecting V_{CE} and I_C for different values of I_B.

Review Questions

1. Add the base and collector currents and compare it with the emitter current and explain the reasons for any deviations.
2. Is the value of h_{FE} constant with variation of collector current ?
3. Does collector current depend on V_{CE} ?

8

LEAKAGE CURRENT OF TRANSISTOR

Theory

When a transistor is connected with emitter open circuited and a reverse potential across its base-collector junction, there can be a leakage current I_{CBO} flowing in the junction. This current changes with temperature, doubling its rate for every 10°C rise. When the transistor is connected in the common-emitter mode with base open circuited, both the emitter-base and base-collector junctions are involved in the leakage current. Assuming that leakage current I_{CBO} flows in the emitter base junction then the same current first flows from base to collector. Due to the current gain of the transistor, the total leakage current $I_{CEO} = I_{CBO} (1+\beta)$ where β is the current gain of the transistor.

Objective

To find the leakage current of the transistor.

Experimental Set Up

Equipments needed

1. Power supply 30V/1A—1 No.
2. Ammeter—1 No.
3. Thermometer—1 No.
4. A brass block with a heating coil to mount the transistor.

Components required

1. Transistor (germanium and silicon)
2. Oil to immerse the transistor.

Procedure

Insert the transistor in the brass block. Take a little quantity of oil in a small container and insert the container in the hole provided in the brass block and immerse the thermometer in the oil. Give connection to the transistor in the common-base configuration. Switch on the supply voltage to the transistor (suitable voltage may be selected depending upon the ratings of the transistor). At the room temperature note down the leakage current. Then heat the oil and note down the leakage current for every 10°C temperature rise. This can be repeated upto 70°C for germanium transistors and upto 100°C for silicon transistors.

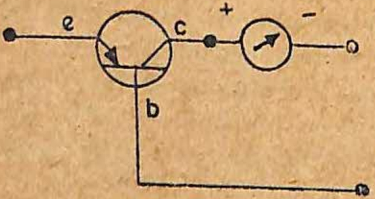


Fig. 8.1

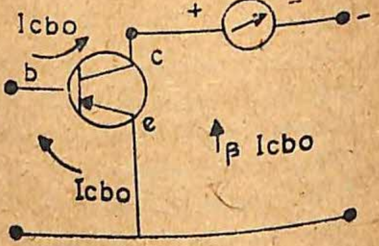


Fig. 8.2

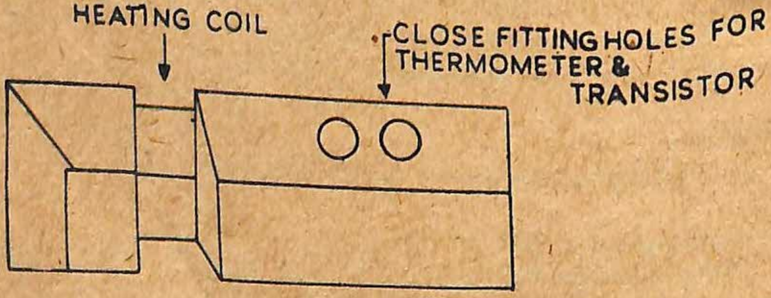


Fig. 8.3

Repeat the experiment for the common-emitter configuration and record the leakage current with rise in temperature. Plot the graph, temperature versus leakage current for both the transistors. The variation of α with respect to temperature can be obtained in the following manner,

$$\beta = \frac{1}{1-\alpha}$$

From the common-emitter readings and common-base readings we can find out the value of β for a particular temperature and α can be computed by using the above equation.

Review Questions

1. What causes the leakage current in a transistor ?
2. Discuss the reasons for higher leakage current in a germanium device.

9

TRANSISTOR BIASING

Theory

Proper biasing of a transistor is a prerequisite for proper operation in the circuitry. This means that the emitter-base junction of the transistor should be forward biased and the collector-base junction reverse biased. For a particular use that the transistor has to be biased to provide the necessary quiescent current and voltages to suit trouble-free operation. The value of the bias current chosen depends upon circuit components. The selection of these components should be such that the transistor is neither in the saturation condition nor cut-off condition when the application is amplification. There are different ways of biasing the base of a transistor to suit various criteria, viz., single resistor bias, voltage divider bias, voltage feedback bias, etc. The stability factor to the various circuits differ and hence depending upon the requirements of this factor in the circuit performance biasing is chosen. The single resistor bias is the simplest of all biasing techniques. This circuit has a built-in instability. Voltage divider bias is more prevalently used circuit when stability factor

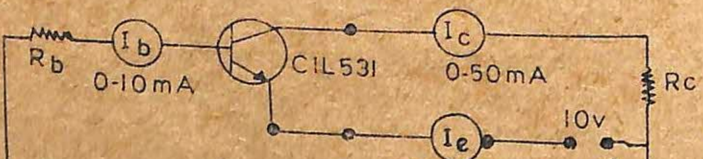


Fig. 9.1

is of prime criterion. The emitter resistor, when added, improves the stability much better. When temperature stability is the purpose, voltage feedback bias is resorted to. Circuit shown in Fig. 9.1 is an example of single resistor bias configuration. The bias current flows through the resistor R_b and then to the base. Depending upon the collector current required, the R_b is chosen. For a collector current of 10 ma and a supply voltage of 10V, the base resistor R_b is calculated in the following manner. The

$$\text{base current required} = \frac{\text{Collector current}}{\text{Current amp. factor}} = I_c/\beta$$

$$\text{Assuming a } \beta \text{ of } 40,\ I_b = \frac{10 \text{ ma}}{40} = 250\ \mu\text{a}.$$

$$R_n = \frac{V_{CC} - V_{BE}}{I_b} = \frac{10-0.7}{250\ \mu\text{a}} = 39 \text{ k}\Omega$$

$$\text{Collector resistance } R_e = \frac{V_{CC}}{10 \text{ ma}} = \frac{10}{10 \text{ ma}} = 1 \text{ K}\Omega.$$

Multiplied leakage current in this type of set-up and its high sensitivity result in bias point instability.

Circuit shown in Fig. 9.2 is an example of voltage divider bias. This arrangement provides reasonably constant base voltage with temperature and serves as a stabler circuit arrangement. For a collector current of 10 ma, the values can be calculated as follows. For the same set of assumptions as in the previous experiment, the base current required is 0.25 ma. There is a voltage drop across R_e. Taking the value of R_e to be, say, 100 ohms, the drop works out to be 1 volt. The base voltage, therefore, should be a minimum of 1.7 volts. Considering Thevenin's equivalent circuit for the base junction and making reasonable assumption of current drain in the chain $R_1 - R_2$, R_2 can be calculated to be

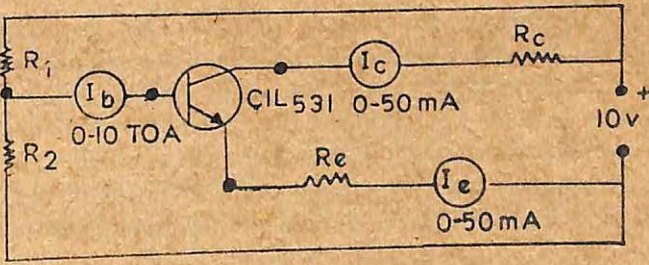


Fig. 9.2

of the order of 680 ohms and R_1 around 3.3 kilo ohms. The value of R_e is $\frac{V_{CC}-(I_cR_e+V_{CE})}{I_c} = 8.8$ kilo ohms. Due to temperature variation V_{BE} changes resulting in change in the bias current and the load current. The emitter resistor R_e and the bias resistor R_1 and R_2 take care of the change in the voltage in reducing the effect of bias current and restoring stability.

The circuit arrangement shown in Fig. 9.3, though gives a low stabitity factor S, it gives a greater versatality in performance in higher temperature. The biasing if done from the collector. instead of from the supply point, whatever voltage variation takes place at the collector gets reflected in to the base resulting in a corrective action. For example if the voltage increases at the collector then there is a corresponding change in the base current, to bring the collector voltage back to its original value. For a collector current of 10 ma and R_e of 100 ohms, the voltage drop across R_e is 1 volt. Base voltage is 1.7 volts.

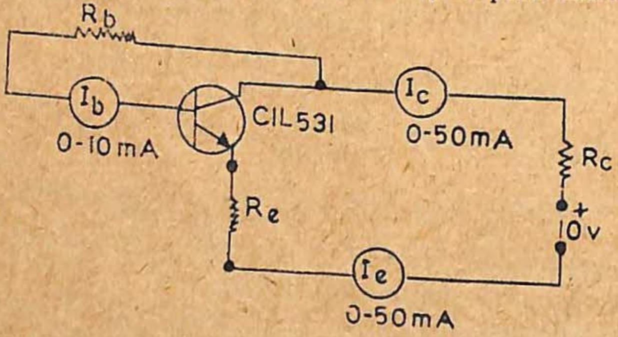


Fig. 9.3

Collector voltage is $V_{CC}-(V_{CE}+I_eR_e)$. For a V_{CE} drop of 1 volt. collector voltage V_C is $10-2=8$ volts.

$$R_b = \frac{8-1.7}{0.25\text{ ma}} = 25\text{ kilo ohms.}$$

$$R_c = \frac{10-8}{10\text{ ma}} = 200\text{ ohms.}$$

Objective

To determine the dc current and voltages in different bias circuits and study their behaviour.

Experimental Set Up

Equipments needed

1. Power supply 30V/4A—1 No.
2. Milliammeter 0-50 ma, dc—2 No.
3. Milliammeter 0-10 ma, dc—1 No.
4. Voltmeter 0-15V, dc—1 No.

Components required

1. Transistor CIL 531 or equivalent—1 Nos.
2. Resistor 100 ohms 10% ¼ W—2 No.
3. Resistor 200 ohms 10% ¼ W—1 No.
4. Resistor 680 ohms 10% ¼ W—1 No.
5. Resistor 1 k. ohm 10% ¼ W—1 No.
6. Resistor 3.3 k. ohms 10% ¼ W—1 No.
7. Resistor 8.8 k. ohms 10% ¼ W—1 No.
8. Resistor 25 k. ohms 10% ¼ W—1 No.
9. Resistor 39 k. ohms 10% ¼ W—1 No.

Procedure

Rig up the circuits shown in Figs. 9.1-9.3. Measure the collector current I_c, emitter current I_e, base current I_b, collector-emitter voltage V_{CE} and tabulate for all the circuits as explained above. Change the value of R_c and study the behaviour of the circuits

Review Questions

1. From the data obtained, calculate the actual value of h_{FE} for the transistor used.
2. Calculate the theoretical values of quiescent currents I_b, I_c and I_e.
3. Compare the theoretical and experimental results.

10

BIAS POINT STABILITY OF A TRANSISTOR UNDER DC CONDITIONS

Theory

The current flowing in a transistor is mainly due to the majority carriers. However, there is an additional small current known as leakage current. This is independent of emitter current and is proportional to temperature variations taking place in the transistor junctions. Due to higher temperature the number of minority carriers increase resulting in the leakage current. The base-emitter voltage which has a negative temperature coefficient also contributes towards the leakage current. The germanium transistors have higher leakage current than that of silicon transistors. Although the leakage current appears to be small as compared to the forward current, it will affect quiescent conditions. The havoc caused by leakage current becomes high at higher temperatures since the thermal component of leakage current doubles for every 10°C rise in temperature. This sudden growth completely changes the biasing conditions. To reduce the sensitivity of the quiescent current to temperature changes, the design of the biasing circuitry should be modified. Controlling of the emitter-base junction voltage has an important bearing in checking the leakage current menace.

Objective

To see the composition of emitter, base and collector currents.

To study the effect of temperature on quiescent values of transistor currents and to observe the role of properly designed biasing circuits.

Experimental Set Up

Equipments needed

1. Power supply 30V/1A—1 No.
2. Milliammeter 0-500 ma—2 Nos.
3. Milliammeter 0-50 ma—1 No.
4. Infrared lamp—1 No.

Components required

1. Transistor AD 149 or equivalent—1 No.
2. Resistor 150 ohms 10% 2W—1 No.
3. Resistor 22 ohms 10% 2W—1 No.
4. Resistor 1 k. ohm 10% ½ W—1 No,
5. Resistor 220 ohms 10% ½ W—1 No.
6. SPDT—1 No.
7. DPDT—1 No.

Procedure

Wire the circuit as shown in Fig. 10.1. Supply 15 volts dc. Observe the collector current. If the current shown is above 400 ma, immediately switch off the power supply. With the emitter switch S_1 open, note the base current and its direction. Reverse the switch S_2 and note the current. This current is the leakage current I_{CBO}.

Close the emitter switch S_1 and reverse the polarity of the meter connected in the base lead. With the supply on, note the values of the three currents. Reduce the value of R_L to 75 ohms by parallelling 150 ohms resistor. Note the readings once again. Due to the presence of the emittor resistance R_e and due to the low values of base biasing resistors, the circuit will remain fairly stable.

A change in temperature will affect the collector current. The transistor should be warmed by using the heating lamp. As the temperature goes up, determine the amount of change in the collector current and leakage current. The placement of the lamp should be such that the transistor does not get excessively heated up. For this, the lamp may be placed about 3 to 4 cms away (this depends upon the voltage of the lamp). The heating should be done for about 5 minutes but the duration may have to be increased if the transistor is placed in good heat sink. With the lamp moved away, note the values of I_C and I_{CBO} quickly and simultaneously (to read I_{CBO}, S_1 should be temporarily opened.

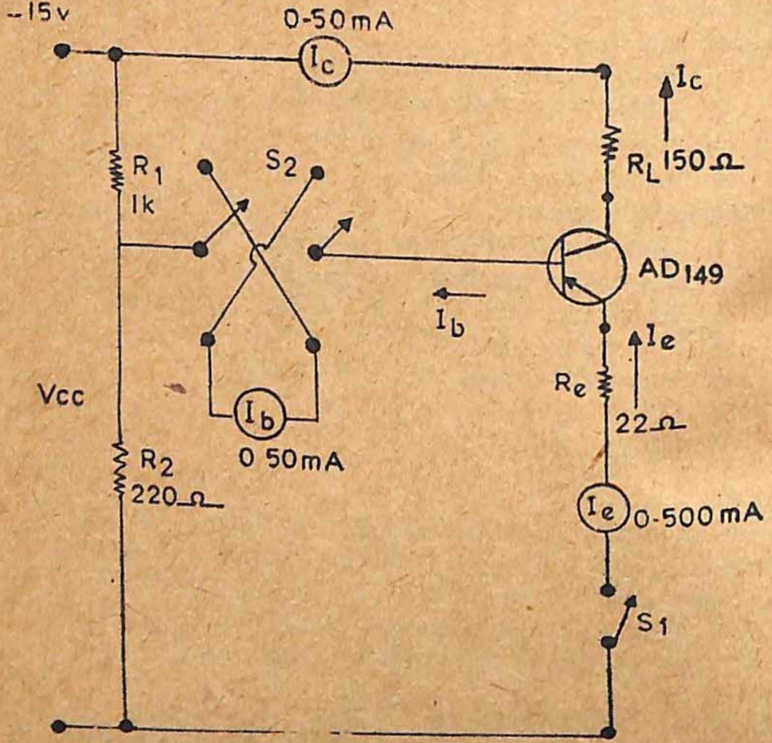


Fig. 10.1

This change in I_{CBO} is due to the change in I_{CO} of the transistor). The two sets of readings of I_C and I_{CBO} determine the stability factor S using the formula

$$S=\frac{\Delta I_C}{\Delta I_{CO}}=\frac{R_e+R_B}{R_e+(1-h_{FB})\,R_B}\text{ where }R_B=\frac{R_1R_2}{R_1+R_2}$$

After cooling off for a period of, say, 10 minutes, repeat the above experiment for a more stable circuit. To increase the stability of the circuit, the base circuit resistance should be reduced keeping the ratio same. For example, R_1 can be reduced to 680 ohms and R_2 to 140 ohms. Since we are interested in the values of I_C and I_{CBO}, these values may only be observed both at ambient and at elevated temperature. Calculate the value of S in this case also and compare this with previously calculated reading. Repeat the experiment for different values of resistors without exceeding the current specifications of the transistor.

Review Questions

1. Explain why the milliammeter in the base should be reversed ?
2. Determine theoretically the quiescent values of base and emitter currents. Explain the difference between the observed and theoretical values, if any.
3. Discuss the factors involved in keeping the stability factor of the transistor stage to acceptable values.

11

SMALL SIGNAL COMMON-EMITTER TRANSISTOR AMPLIFIER

Theory

Common-emitter amplifier is widely used in electronic circuits for amplification purposes. Transistors being a current device, input resistance of the transistor amplifier is low. Large coupling capacitors must be used for good frequency response and for good phase shift performances at low frequencies. A typical common-emitter amplifier is designed for the following specifications. (*i*) Frequency response 20 Hz to 100 kHz, (*ii*) Load resistance 4.7 kilo ohms, (*iii*) Input impedance 60 k. ohms. (*iv*) Voltage gain 20, (*v*) Source characteristic impedance 60 ohms and (*vi*) Supply voltage + 15 volts. Choose a *npn* transistor having good gain band width products. One such transistor is CIL 531. This is used in this design. This being a silicon transistor, it has got good temperature stability.

The collector resistance R_c is chosen for a collector current of 1.5 ma. The drop across R_c is therefore 7 volts. The quiescent dc voltage at the collector is 8 volts. The input impedance of the transistor depends on the emitter resistance. The approximate value of input resistance is equal to $h_{FE}.R_1$. The h_{FE} of the transistor is 120. Hence, the value of R_1 is 0.5 kilo ohm. The emitter bypassing capacitor is chosen to give low reactance at the lowest frequency. The reactance of the capacitor at the lowest frequency of 20 Hz should be around 1/10 of the emitter resistance. An electrolytic capacitor of value 50 mfd will give low impedance path at this frequency. The base current required is 12.5 ma. The drain current in the bias circuit could be 5 times the base current for reducing the loading effect. Choosing a drain current of 62.5 ma, the value of (R_2+R_3) will be 240 kilo ohms. Base voltage at B is 1.5 volts. This means the value of $R_3 = \frac{1.5 \times (R_2+R_3)}{V_{CC}}$. This works out to be 24 kilo ohms. A practical value of 27 kilo ohms is chosen. The capacitor C_b is chosen to be as 0.1 mfd.

Objective

To determine the frequency response, voltage gain and input and output resistances of the common-emitter amplifier.

Experimental Set Up

Equipments needed

1. Oscilloscope—1 No.
2. Sinewave oscillator—1 No.
3. Frequency counter—1 No.
4. Power supply 30V/1A—1 No.
5. Variable resistance box—1 No.

Components required

1. Transistor CIL 531 or equivalent—1 No.
2. Capacitor (electrolytic) 50 mfd/15V—1 No.
3. Capacitor (polyster) 0.1 mfd—1 No.
4. Resistor 470 ohms 10% ¼ W—1 No
5. Resistor, 4.7 K, 10 K, 27K, 220K, 10% ¼ W—1 No. each.

Procedure

Give connection as shown in Fig. 11.3. Set the oscillator output around 10 milli volt at 10 Hz. Measure the same using an oscilloscope and note down the values. Measure the output of the amplifier after connecting the oscillator to the input of the amplifier. Keeping the oscillator output at a constant value of 10 mv, vary the output frequency from 10 Hz upwards in suitable steps of frequency upto 120 kHz. In each of the voltage setting and frequency setting note down the output of the amplifier in the oscilloscope. Draw a graph connecting the frequency on the voltage gain (voltage gain $A = V_{\text{output}}/V_{\text{input}}$).

Find out the $-3dB$ point from the graph ($-3dB$ point corresponds to the gain at 0.707 of the mid band gain). Frequencies

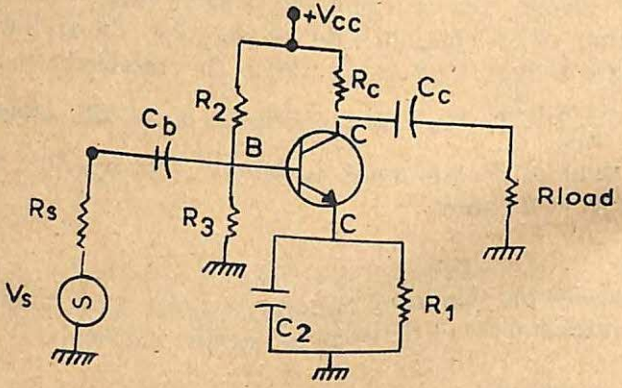


Fig. 11.1

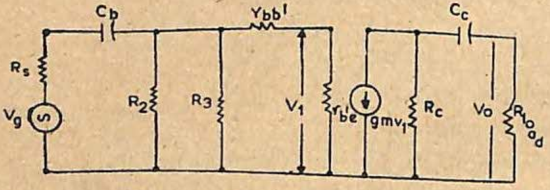


Fig. 11.2

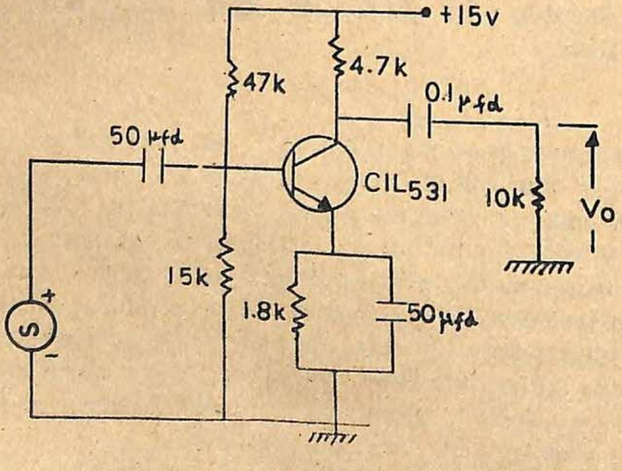


Fig. 11.3

between the $-3dB$ points correspond to frequency response of the amplifier. Connect a variable resistance box in series with the oscillator and vary the resistance till the output reduces to 50% of its value before the resistance box was introduced for a constant input of 10 mv at 1 kHz. Note the value of the resistance in the resistance box which corresponds to input impedance of the amplifier. Remove the load resistance and the variable resistance box from the circuit. Note down the output voltage of the amplifier for an input of above-mentioned quantities. Then connect the resistance box in the place of load resistance and vary its resistance till the output voltage comes down to 50% of its open circuit value. This value of the resistance in the resistance box corresponds to the output impedance of the amplifier.

Repeat the experiment for different gains by varying the value of collector resistance R_C.

Review Questions

1. Explain the alpha cut-off frequency of the amplifier.
2. How does the supply voltage variation affect the amplifier performance.

12

EMITTER FOLLOWER

Theory

Emitter follower is very useful circuit widely used for impedance matching. Emitter follower has got high input impedance and very low output impedance. This property ideally suits the input and output stages of multistage amplifier circuits. It has got good stability. A typical circuit is shown in Fig. 12.1.

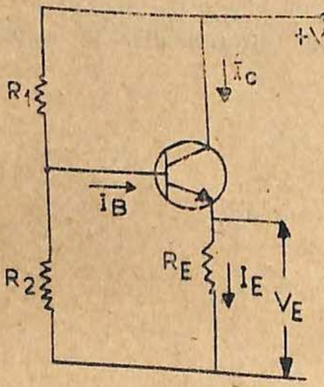


Fig. 12.1 (a)

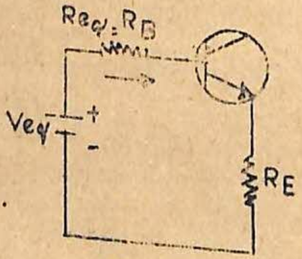


Fig. 12.1 (b)

The circuit shown in Fig. 12.1(a) can be analysed for a collector current of 1 ma, V_{CE} of 10 V, stability factor $S=5$ and $V_{CC}=20$ V. Assuming that I_E is almost equal to I_C, emitter voltage V_E is 10 V. Therefore $R_E=V_E/I_E=10$ k. ohms,

$$I_B=\frac{1}{\beta_{DC}}\left[I_C-(1+\beta_{DC})I_{CBO}\right].$$

If we assume the value of β_{DC} as 100 and I_{CBO} as zero (for silicon transistors, the value of I_{CBO} is negligible), $I_B = I_C/\beta_{DC} = 0.01$ ma. Stability factor $S = \dfrac{R_E + R_B}{R_E + \dfrac{R_B}{\beta_{DC}+1}}$ where R_B is the Thevenin's equivalent resistance in the base circuit. Substituting for R_E and S, $R_B = 42$ k. ohms. Base emitter voltage drop for a silicon transistor varies from 0.5 V to 0.7 V. Assuming a typical value of 0.5 volt, we get V_{EQ} in Fig. 12.1 (b) as $V_E + V_{BE} = 10 + 0.7$. V_{eq} is therefore equals to 10.7 V.

$$R_B = R_1.R_2/R_1 + R_2.$$

$$R_2/R_1 + R_2 \times V_{CC} = V_{eq}.$$

Therefore $R_2/R_1 + R_2 = V_{eq}/V_{CC} = 10.7/20$, i.e., the approximate value of R_1 and R_2 are 77 k. ohms and 93 k. ohms respectively.

Input impedance $Z_i \cong \dfrac{(r_e + R_E)(r_c + R_L)}{(r_c/1+\beta) + R_L}$

Since $R_C/1+\beta \gg R_L$, $Z_i = (1+\beta)(r_e + R_E)$ where r_e is the emitter resistance of the transistor. From the diode equation r_e is approximated in ohms in the following manner, r_e (in ohm) is equal to 26 mv/I_e (ma).

In the circuit R_E is far greater than r_e. This leads us to the equation of input impedance, $Z_i = (1+\beta)R_E$. From the circuit value $Z_i = (1+100) \times 10$ kilo ohms. This input impedance realised in the circuit is much less than the theoretical value because R_2 is smaller and comes in parallel to the input circuit.

The output impedance $Z_o = \dfrac{1}{\dfrac{1}{R_L} + h_{oc}}$

Objective

To determine the voltage gain, frequency response, input resistance and output impedance of the emitter follower.

Experimental Set Up

Equipments needed

1. Oscilloscope—1 No.
2. Sinewave oscillator—1 No.
3. Power supply 30V/1 A—1 No.
4. Frequency counter—1 No.
5. Variable resistance box—1 No.

Components required

1. Transistor CIL 532 or equivalent—1 No.
2. Resistance 10 k, ohms 10% ¼ W—1 No.
3. Resistance 80 k. ohms 10% ¼ W—1 No.
4. Resistance 100 k. ohms 10% ¼ W—1 No.
5. Capacitor (Polyster or mica) 0.01 mfd—1 No.

Procedure

Rig up the circuit as shown in Fig. 12.2. Keep the sinewave oscillator output at 1 V around a frequency of 1 kHz and monitor the output of the emitter follower. Vary the input frequency in suitable steps keeping oscillator output voltage as constant and monitor the output of the emitter follower. Determine the input and output impedances as per the procedure laid down in experiment No. 11.

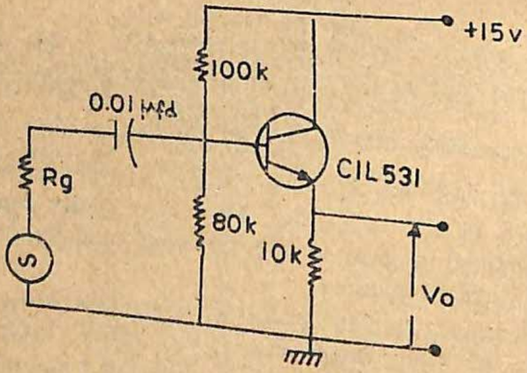


Fig. 12.2

Review Questions

1. What are the factors which determine the input impedance of the emitter follower ? Explain the differences in the actual value of the input impedance of the circuit as compared to theoretically calculated value.
2. Explain the reason for the voltage gain to be less than unity.

13

DIRECT COUPLED AMPLIFIER

Theory

Direct coupled amplifier can only be the answer for very low frequency applications. Advantages of this amplifier circuit are that it does not limit the low frequency response or allows low frequency phase shift. Quiescent output voltages of the preceding stage provides input bias to subsequent stages. However, the feedback around several stages can lead the bias stability factor S to less than unity. A two stage direct coupled common emitter amplifier is considered. Transistors chosen are CIL-531 or their equivalent. The supply voltage is kept at 15V dc. Making the following assumptions the design of the amplifier is carried out for maximum output.

Let $I_{C_1} = 1$ ma $R_{E_1} = R_{E_2} = 2.2$ k. ohms and $R_2 = 10$ k. ohms respectively.

$I_{C_2} = 2$ma $C_{E_1} = C_{E_2} = 100$ mfd.

Using the approximate design procedures $V_{E_1} \approx I_{C_1} \times R_{E_1}$

$= 0.001 \times 2200$

This works out to be 2.2 V

$V_{B_1} = V_{E_1} + V_{BE_1} = 2{\cdot}2 + 0.6 = 2.8$ V.

$V_{CC} = 15$ V

$VB_1 = V_{CC} \times R_2/R_1 + R_2$.

$R_1 + R_2$ is approximately $= 53.5$ k. ohms. Since R_2 is already chosen as 10 k. ohms, R_2 becomes 43.5 k. ohms. Since there is no value in this range, a 47 k. ohms resistor is chosen for this purpose. The base current required $= I_{C_1}/\beta = 1$ ma$/60 = 16.6$ micro amperes. Therefore, the bias arrangement will be in a position to supply the required base current without loading the circuit.

$V_{E_2} \approx I_{C_2} \times R_{E_2} = 0.002 \times 2200 = 4.4$ V.

$V_{B_2} = 4.4 + 0.6 = 5$ V

R_{C_1} can be determined in the following manner.

$V_{CC} = I_{C_1} \times R_{C_1} + V_{B_2}$

$V_{C_1} \times R_{C_1} = V_{CC} - V_{B_2} = 15-5$

$R_{C_1} = 10$ k. ohms

The choice of R_{C_2} is based on the requirement for developing the maximum output. The maximum swing in collector voltage V_{C_2} is, V_{C_2} min. $= V_{E_2} + V_{CE}$ min.

V_{CE} min. is the minimum voltage across collector emitter of the transistor for the proper transistor operation and this is assumed to be 1 volt for the transistor chosen.

Therefore V_{C_2} minimum $= 4.4 + 1 = 5.4$ V.

When the transistor is nearly cut off, V_{C_2} max. is equal to 15 V.

Therefore the collector voltage may swing from 5.4 volts to 15 volts with a quiescent level of 10.2 volts. The peak to peak swing is 9.6 volts and the peak swing is 4.8 volts.

$R_{C_2} \times I_{C_2} = 4.8$ V.

$R_{C_2} = 4.8$ V/2 ma $= 2.4$ k. ohms.

The circuit values are calculated as detailed above.

Objective

To study the characteristics of direct coupled amplifier.

Experimental Set Up

Equipments needed

1. **Audio oscillator—1 No.**
2. **Power supply 30 V/1 A—1 No.**
3. **Oscilloscope or VTVM—1 No.**

Components required

1. Transistor CIL 531 or equivalent—2 Nos.
2. Resistor 2.2 k. ohms 10% ½ W—2 Nos.
3. Resistor 2.4 k. ohms 10% ¼ W—1 No.
4. Resistor 10 k. ohms 10% ¼ W—2 Nos.
5. Resistor 47 k. ohms 10% ¼ W—1 No.
6. Capacitor (Electrolytic) 100 mfd/15V—4 Nos.

Procedure

Connect the circuit as shown in Fig. 13.1 and insert the values of components as derived in the design procedure. Feed the signal of amplitude 100 mv at 10 Hz and find out the output. Vary the frequency from very low value and determine frequency response. Find out the lowest frequency to which the amplifier. is in a position to respond satisfactorily. Increase the value of C_1 and determine the lowest frequency. Find out input and output impedance of the circuit.

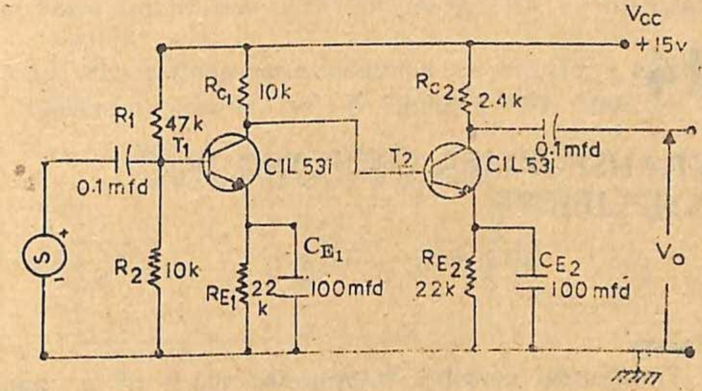


Fig. 13.1

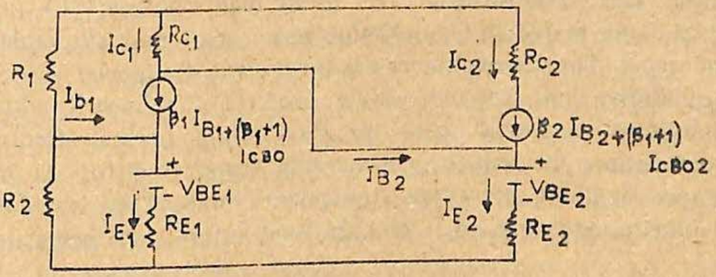


Fig. 13.2

Review Questions

1. Calculate the theoretical values of input and output impedances of the amplifier and compare it with practical values. Explain their differences, if any.
2. How the stability of the dc amplifier is ensured in the circuit ?

14

TRANSFORMER COUPLING IN AMPLIFIERS

Theory

Transformer coupling between the stages of a transistor amplifier gives some significant advantages and some disadvantages. The advantages are (*i*) good bias stability, (*ii*) simple impedance matching for optimum power gain, and (*iii*) isolation of stages. The disadvantages are (*a*) limited frequency response, (*b*) relative high cost and weight, and (*c*) nonlinearily due to nonlinear magnetic core property. For limited frequency applications the transformer coupling is preferred for its impedance matching advantage. Equivalent circuit of the transformer is illustrated in Fig. 14.1. The idealised output transformer gives

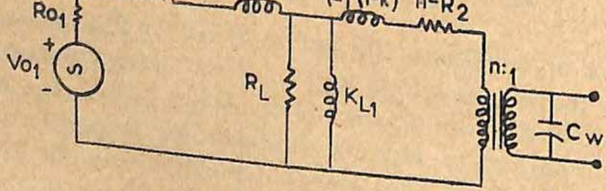


Fig. 14.1

the required impedance matching at the output terminals.

R_1 = Primary dc resistance, R_{O_1} = Source point impedance.

R_2 = Secondary dc resistance, V_{O_1} = Source voltage.

n = Primary/secondary turns ratio.

L_1 = Primary inductance.

K = Coefficient of coupling of primary to secondary.

KL_1 = Mutual inductance, primary to secondary.

$(1-K) L_1$ = Leakage inductance, primary to secondary.

R_L = Equivalent core loss resistor.

C_W = Equivalent distributed capacitance referred to secondary winding.

Analysing the low frequency response we can write for a reasonably efficient transformer of K approximately equal to 1,

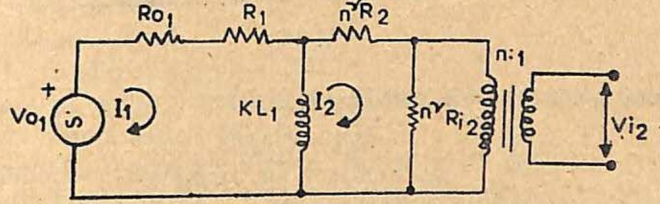


Fig. 14.2

$WL_1 (1-K)$ far less than R_1. At very low frequency, W being small, series inductance may be neglected. In the same manner, the term R_L may also be ignored in comparison with the reactance of KL_1. The capacitive reactance of C_W becomes very large and may be neglected. The simplified equivalent circuit is as shown in Fig. 14.2. Writing down the output and input voltage ratio and simplifying the relationship for the frequency where attenuation begins to level off with increasing frequency is

In the mid-frequency region the equivalent circuit gets modified as shown in Fig. 14.3. Frequency response is flat in

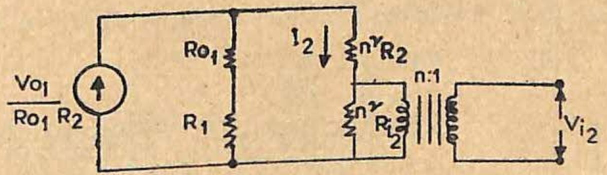


Fig. 14.3

this region, which is generally useful operating region of the transistor amplifier. The high frequency region of the frequency-response curve is influenced by series inductor $L_1 (1-K)$. The shunt inductor KL_1 offers very high reactance at high frequency and so is neglected. Equivalent circuit for high frequency condition is shown in Fig. 14.4. Neglecting capacitor C_W, equivalent

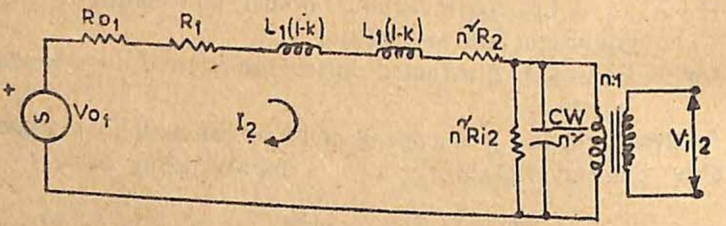


Fig. 14.4

circuit gives the time constant L/R as

$$\frac{L}{R}=\frac{2(1-K)L_1}{R_{o_1}+R_1+n^2\,(R_{i_2}+R_2)}$$

Corresponding frequency to this time constant is

$$W=\frac{R_{o_1}+R_1+n^2\,(R_{i_2}+R_2)}{2(1-k)L_1}$$

If C_W is not ignored the circuit gives rise to a series resonance with equivalent transformer leakage reactance somewhere in the high frequency region. This causes a hump in the frequency response characteristic in the high frequency side. The amplitude of this hump depends on Q of the circuit. For a matching transformer $n=\sqrt{\frac{R_S}{R_L}}$ where R_S and R_L are the driving and load impedances respectively. The relationship between W_L, R_S and L_1 is

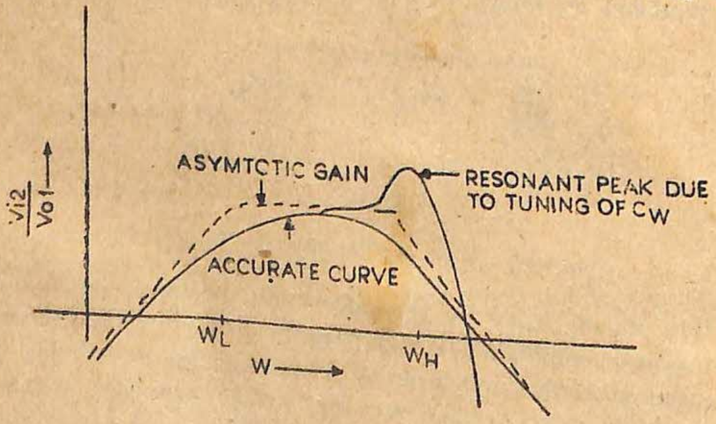


Fig. 14.5

given by $L_1 = \frac{R_S}{2W_L}$. Frequency response characteristic of a transformer coupled amplifier is as shown in Fig. 14.5.

Objective

To find the frequency response of a transformer coupled amplifier.

Experimental Set Up

Equipments needed

1. Audio oscillator—1 No.
2. AC millivoltmeter or a CRO – 1 No.
3. Power supply 30V/1A—1 No.

Components required

1. Transistor CIL 531 or equivalent—1 No.
2. Suitable transformer—1 No.
3. Resistor 10 k. ohms 10% ¼ W—1 No.
4. Resistor 5.6 k. ohms 10% ¼ W—1 No.
5. Resistor 10 ohms 10% ¼ W—1 No.
6. Capacitor 25 mfd/10V—1 No.

Procedure

For a collector current of 5 ma (or suitable value depending upon the transformer and transistor capability), choose the value of R_E as 1 k. ohm to give sufficiently good stability. The base voltage V_B should, therefore, be equal to 5.6 volts.

$$V_B = \frac{R_2 \times V_{CC}}{R_1 + R_2}, \text{ i.e., } 5.6. = \frac{R_2 \times V_{CC}}{R_1 + R_2}$$

Taking in to consideration the β of the transistor as 60, R_1 can be

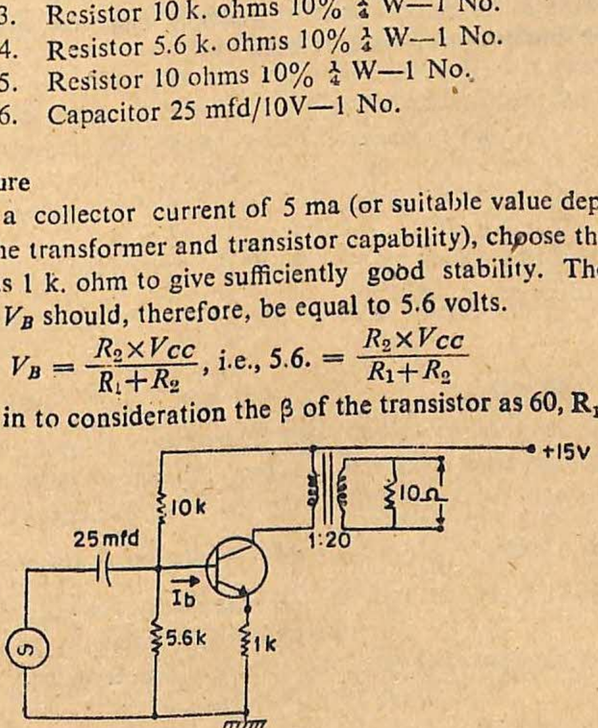


Fig. 14.6

fixed as 10 k. ohms, then $R_2 = 5.6$ k. ohms. For the lowest frequency of 10 radians/sec., time-constant RC should be 0.1, such that $(R_1 \parallel R_2)\, C_1 = 1/10$. Therefore $C_1 = 25$ mfd. Connect the circuit as shown in the Fig. 14.6 and vary the input frequency from the audio oscillator, keeping the amplitude constant at all the frequencies. Note the output voltage and draw the relationship between the input frequency and voltage gain, $\frac{V_o}{V_i}$ (refer Fig. 14.5)

Review Questions

1. Explain the impedance matching characteristics of an audio frequency transformer used in this experiment.
2. How does the frequency response of the transformer affect the overall frequency response of the amplifier ?
3. Describe the precautions to be taken in the winding of the transformer for increasing the frequency response subject to the limitations of the core used in it.

15

TUNED AMPLIFIER

Theory

Whenever it is required to amplify a narrow band of frequencies and reject signals of higher and lower frequencies, tuned amplifiers or narrow band amplifiers are used. A tank circuit using L-C components is used as the load in the amplifier circuit. This parallel L-C circuit is tuned to mid-frequency. Depending upon the band of frequency required, the Q of the tank circuit is chosen. An ideal tuned circuit is shown in Fig. 15.1.

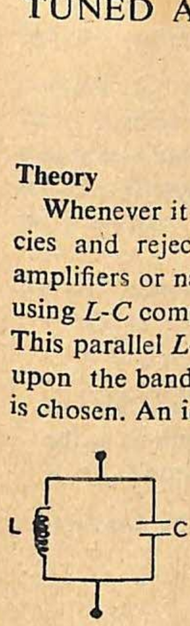


Fig. 15.1

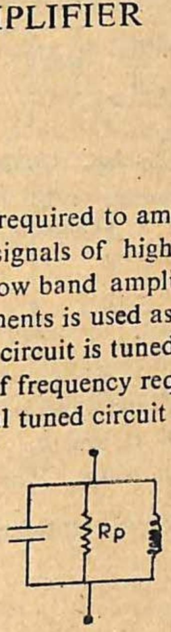


Fig. 15.2

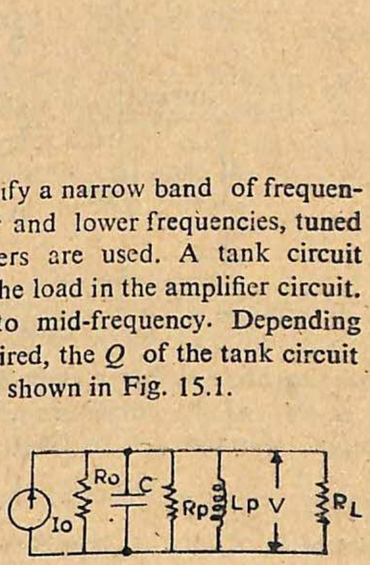


Fig. 15.3

Here L and C components are considered as ideal, that is L has no series resistance and C has infinite resistance across it. The Q or figure of merit of a coil is defined as the ratio of inductive reactance to resistance. That is $Q = \frac{X_L}{R_s}$, where X_L indicates the inductive reactance and R_s that of the leakage resistance. This means in physical terms

$$Q = 2 \frac{\text{energy stored in electric and magnetic field per cycle}}{\text{energy dissipated per cycle}}$$

The tank circuit as shown in Fig. 15.1 can be rewritten as in Fig. 15.2 for practical components values. The resistance shown in the circuit is given by the equation $R_p = R_s(1+Q^2)$. For a typical value of $Q = 100$ and $R_s = 10$ ohms, R_p will be approximately equal to 100 kilo ohms. When a tuned circuit is loaded, the power transferred to the load can be determined by the equation,

$$P_L\,(\text{ideal}) = \frac{V^2}{R_L} = \frac{I_0^2 \times R^2}{R_L}.$$

Referring to Fig. 15.3 and assuming R_p to be infinite, the power equation as shown above is found effective. The value of R is the parallel combination of R_o and R_L, where R_o is the output resistance of a transistor stage. The circuit Q is $\frac{1}{(G_o+G_P+G_L)\times p}$, where G_o, G_p and G_L represent the conductance of R_o, R_p and R_L respectively.

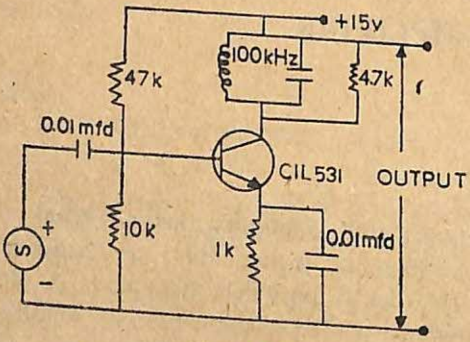


Fig. 15.4

Objective

To study the performance of a tuned amplifier.

Experimental Set Up

Equipments needed

1. Power supply 30V/1A—1 No.
2. CRO—1 No.
3. RC oscillator—1 No.

Components required

1. Transistor CIL 531 or equivalent—1 No.
2. Resistor 1 kilo ohm 10% ¼ W—1 No.
3. Resistor 4.7 kilo ohms 10% ¼ W—1 No.
4. Resistor 10 kilo ohms 10% ¼ W—1 No.

5. Resistor 47 kilo ohms 10% $\frac{1}{4}$ W—1 No.
6. Capacitor (Polyster) 0.01 mfd—2 Nos.

Procedure

Connect the circuit as shown in the Fig. 15.4. The tank circuit is chosen for a mid-frequency of 100 kHz with a Q of 100. The design of the tank circuit is carried out as explained in theory. Vary the signal input around 100 kHz and measure the output in the CRO at half power points. Calculate the value of Q from the observations using the formula $Q = \frac{\text{centre frequency}}{f}$, where f stands for the difference in frequency between the higher and lower half power points about central frequency. Compare the theoretical and actual values of Q. For different tank circuits at different frequency repeat the experiment and study the theoretical and actual values of Q.

Review Questions

1. Explain the impact of loading on the Q of the tank circuit.
2. How does the frequency limitation of the transistor affect the performance of this circuit ?

16

HIGH INPUT IMPEDANCE TRANSISTOR AMPLIFIER

Theory

Input impedance of a transistor amplifier is generally low. This causes loading effects on the previous stages. With suitable design technique a high input impedance circuit can be realised. For a transistor having the following specifications, $h_{ib} = 75$ ohms, $h_{ob} = 1 \times 10^{-6}$ mho, $h_{rb} = 10 \times 10^{-4}$ and $h_{fb} = -0.98$, a design is undertaken to achieve an input impedance of 100 kilo ohms. The load to be fed is assumed to be 10 kilo ohms. Taking a common-emitter configuration the various resistor values are calculated. From the expression for input impedance,

$$h_{ib} + R_e = \frac{R_i(h_{ob} \times R_L + 1 + h_{fb}) + h_{rb}\, h_{fb}\, R_L}{1 + h_{ob}\,(R_L - R_i)}$$

This is approximately equal to 3300 ohms. Therefore $R_e = 3225$

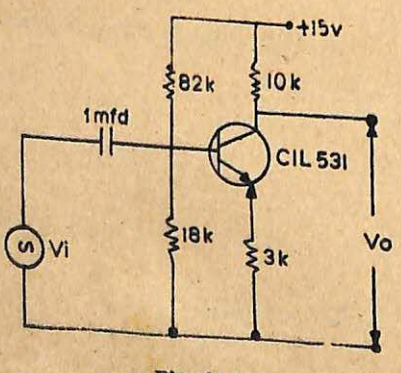


Fig. 16.1

ohms. For a collector current of 1 ma, biasing resistances are calculated in the following manner. Since I_C is approximately equal to I_E, the drop across R_e is equal to 3.225 volts. Therefore, the base voltage should be 3.825 volts. Since β of the transistor is approximately 50, base current is 20 micro amperes. A total current of 200 micro amperes through R_1 and R_2 (Fig. 1.61) will be sufficient to provide the base current without loading the circuit. Hence $R_1+R_2 = \frac{V_{CC}}{I_B}$. For a V_{CC} of 20 volts, R_1+R_2 = 100 kilo ohms. Voltage $V_B = \frac{V_{CC}\times R_2}{(R_1+R_2)}$. R_1 and R_2 are chosen as 82 and 18 kilo ohms respectively.

Objective

To study the high input impedance amplifier characteristics.

Experimental Set Up

Equipments needed

1. Audio oscillator—1 No.
2. CRO or ac Millivoltmeter—1 No.
3. Power supply 30V/1A—1 No.

Components required

1. Transistor CIL 531 or equivalent—1 No.
2. Resistor 3 kilo ohms 10% $\frac{1}{4}$ W—1 No.
3. Resistor 10 kilo ohms 10% $\frac{1}{4}$ W—1 No.
4. Resistor 18 kilo ohms 10% $\frac{1}{4}$ W—1 No.
5. Resistor 12 kilo ohms 10% $\frac{1}{4}$ W—1 No.
6. Capacitor (Mica) 1 mfd—1 No.

Procedure

Connect the circuit as shown in the Fig. 16.1. Find out the frequency response, input and output impedance as explained in the previous experiments.

Review Questions

1. Compare the value of the input impedances obtained with the theoretical value. Explain the reasons for the differences, if any.

17

DIFFERENTIAL AMPLIFIER

Theory

Differential amplifier is widely used in instrumentation circuits. It is called as differential amplifier because its output voltage is proportional to the difference of two voltages supplied to its two separate inputs. Two transistors are necessary for this. When the transistors are well matched, the output voltage taken between the collectors, is independent of parameter changes or changes in the value of leakage current of either of the transistor. Two inputs are shown as V_1 and V_2 in Fig. 17.1. The circuit will amplify only if there exists a difference between the input voltages. When V_1 and V_2 are equal, that is when the inputs are common, an ideal amplifier should give zero output. This means that the common mode voltage is completely rejected at the output. For an ideal amplifier the common mode rejection ratio (CMRR) should be infinite. Due to various limitations such as matching of the transistors, aging of the components, etc., CMRR cannot be achieved to the near ideal condition. So a differential amplifier is considered to be good if the CMRR is above 80 dB. The advent of integrated circuit has helped in realising differential amplifier with CMRR of 120 dB and more. Writing down the Kirchhoff's equations for the circuit, the output voltage V_o can be written as $V_o = \frac{(V_1 - V_2)\,\beta . R_L}{R_s + (\beta+1)\, r_e}$, where V_1 and V_2 are the input voltage shown in Fig. 17.1, β is the ac current amplification factor of the transistor, R_L is the load resistance, R_s is the equivalent lumped resistance of the generator and r_e is the emitter resistance of the transistor.

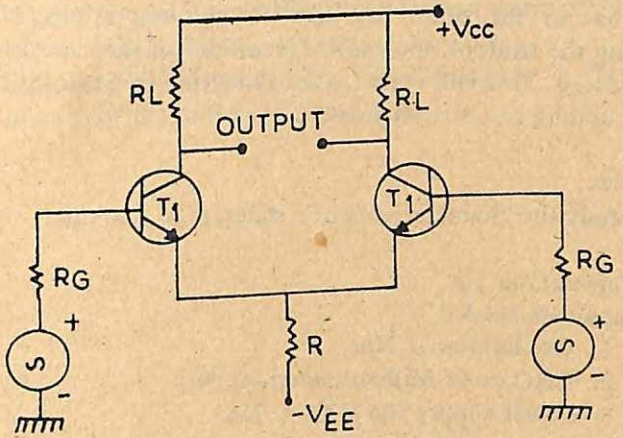


Fig. 17.1

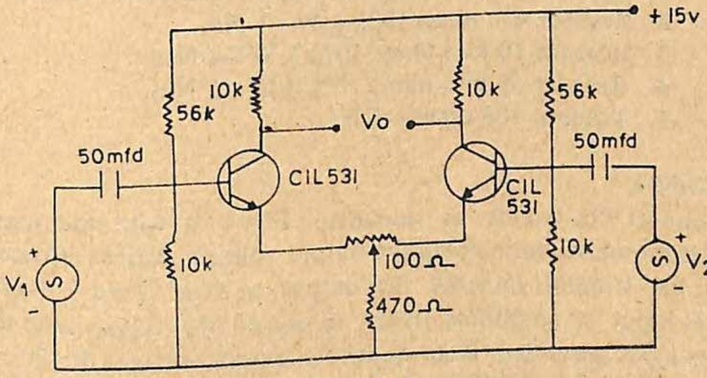


Fig. 17.2

A single power supply differential amplifier is given in Fig. 17.2. The dc current under quiesecent conditions is adjusted around 1 ma, if necessary using the trimpot. The base bias resistors provide the necessary bias and base currents to keep the transistor in operating condition. When the transistors and the resistors are well matched the output measured across the collectors will be zero volt. The imperfections in the matching of transistors could lead to a difference in the output even when the input voltage are grounded or kept at zero. (By adjusting the emitter trimpot, the current in the transistors are slightly detuned to achieve the zero output condition. For example, if the value of β of one of the transistors is more than the other, the collector current corresponding this transistor will be more than that of the other for identical bias conditions. Now by adjusting the trimpot, the emitter resistance of the transistor can be increased. This will result in the reduction of collector current corresponding to the transistor.)

Objective

To study the characteristics of a differential amplifier.

Experimental Set Up

Equipments needed

1. Oscillators—2 Nos.
2. CRO or ac Millivoltmeter—1 No.
3. Power supply 30V/1A—1 No.

Components required

1. Transistor CIL 531 (matched) or equivalent—2 Nos.
2. Resistor 470 ohms 10% $\frac{1}{4}$ W—1 No.
3. Resistor 10 kilo ohms 10% $\frac{1}{4}$ W—4 Nos.
4. Resistor 56 kilo ohms 10% $\frac{1}{4}$ W—2 Nos.
5. Trimpot 100 ohms—1 No.

Procedure

Connect the circuit as shown in Fig. 17.2 with the input points grounded, note down the output voltage. Adjust, if necessary, the trimpot to bring the output to zero. Feed a 1 kHz signal input of amplitude 10 mv to one of the inputs with the other input grounded. Note down the output voltage. Find out the gain of the amplifier. Repeat the experiment keeping this input at the ground level and feeding these signal at the other input. Feed signal at both the inputs such that there is a difference of at least 10 mv between the inputs and note down the output. The above experiment can be repeated for different frequencies.

Review Questions

1. Calculate the common mode rejection ratio of the symmetric amplifier, $(\text{CMRR}) = \dfrac{\text{Differential mode gain}}{\text{Common mode gain}}$
2. Differential amplifiers are used as the input stage of opera-

tional amplifiers. In this function one of the differential inputs is used as a feedback connection and other as the signal input. Discuss the reasons for this.

3. Discuss the effect of aging of components in the performance of the differential amplifier.

18

NEGATIVE FEEDBACK AMPLIFIER

Theory

The concept of feedback is gainfully exploited in amplifier design to achieve higher stability, better frequency response, higher input impedance and lower output impedance at the cost of gain. The above properties are obtained by suitably feeding back a portion of the output signal to its input in suitable phase relation. When feedback takes place the properties of the amplifier change very much from those of the original amplifier.

In its simplest form, the effect of feedback can be understood with the help of the block diagram shown in Fig. 18.1. The block *A* denotes the amplifier and the block *B* denotes the feedback network. The voltage relations can be written down in the following manner:

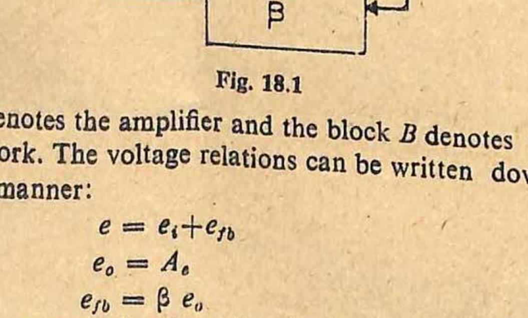


Fig. 18.1

$$e = e_i + e_{fb} \tag{1}$$

$$e_o = A_e \tag{2}$$

$$e_{fb} = \beta\, e_o \tag{3}$$

The voltage e_{fb} is the signal feedback in the circuit. The new gain of the feedback amplifier, A_{fb} can be written as

$$A_{fb} = \frac{e_o}{e_i} \tag{4}$$

$$e_o = \frac{A.e_i}{1-A\,\beta} \tag{5}$$

Therefore, $$A_{fb} = \frac{A}{1-A\,\beta} \tag{6}$$

The amount of feedback can be written in quantitative form using decibels, dB of feedback

$$= 20 \log_{10} \left| \frac{1}{1-A\,\beta} \right|$$

$$= -20 \log \mid 1-A\beta \mid \tag{7}$$

The feedback is negative or degenerative when $\mid 1-A\beta \mid < 1$. When $(1-A\beta)$ is real, it means that $A\beta < 0$. The feedback is positive or degenerative when $\mid 1-A\beta \mid \geqslant 1$. When $A\beta = +1$, the closed loop gain becomes infinite. This means that the feedback amplifier goes into oscillation. Thus an amplifier employing feedback should be closely examined for the presence of any instability.

The fractional change in the gain can be expressed as $\frac{dA}{A}$. In turn, this will cause a change in the gain of the feedback amplifier, which is denoted as $\frac{dA_{fb}}{A_{fb}}$. Differentiating the equation (4), we get,

$$\frac{dA_{fb}}{dA} = \frac{1}{(1-A\beta)^2}$$

$$= \frac{A}{(1-A\beta)} \frac{1}{(1-A\beta)} \frac{1}{A}$$

The fractional change can be related as

$$\frac{dA_{fb}}{A_{fb}} = \frac{1}{1-A\beta} \cdot \frac{dA}{A} \tag{8}$$

This means that the negative feedback reduces the effects of parameter variation. That is the negative feedback stabilises the gain and the positive feedback causes instability and oscillation. Similarly, it can be shown that feedback can alter impedance levels and frequency response.

Objective

To study the effects of negative feedback.

Experimental Set Up

Equipments needed

1. ac millivoltmeter—1 No.
2. Audio oscillator—1 No.
3. Decade resistance box—1 No.
4. CRO—1 No.
5. Power supply 30V/1A—1 No.

Components required

1. Transistor CIL 531 or equivalent—1 No.
2. Resistor 4.7 kilo ohms 10% $\frac{1}{4}$ W—1 No.
3. Resistor 18 kilo ohms 10% $\frac{1}{4}$ W—1 No.
4. Resistor 47 kilo ohms 10% $\frac{1}{4}$ W –1 No.
5. Capacitor 8 mfd/10V–1 No.
6. Capacitor 8 mfd/25V–1 No.
7. Capacitor 50 mfd/10V–1 No.

Procedure

Set up the circuit as shown in Fig. 18.2 and put the switch in the decade resistance box in position 1 such that the resistance in the emitter circuit is about 4.7 kilo ohms. Feed a signal of 1 kHz from the audio oscillator and measure the output at *D*. The level of the input is adjusted such as to overcome

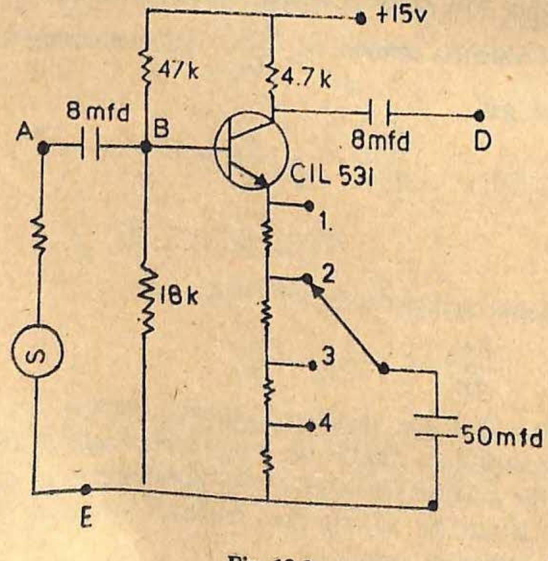


Fig. 18.2

any noice but small enough not to overload the stage, say, around 1 volt. By measuring the amplitudes of the signals at input and output, determine the gain as e_o/e_i. Vary the input signal frequency and determine the frequency response, input impedance and output impedance as explained in the previous experiments. Change the value of the emitter resistance in suitable steps and determine the above-mentioned parameters. Compare the characterstics for different feedback ratios from the above observations.

Review Questions

1. Determine the voltage gain of the amplifier under conditions of no feedback and negative feedback.
2. What effect the introduction of the negative feedback has on the linearity of the amplifier ?
3. How does the bandwidth of the amplifier with negative feedback compare with bandwidth of the amplifier without feedback ?

19

TRANSISTOR AMPLIFIER–SIGNAL LIMITATIONS

Theory

The realisable gains—current, voltage or power—of any transistor circuit is always less than that available from the transistor itself. This is because the external circuitry incorporated reduces the gain. In the common emitter circuit the reduction in the gain is as a result of the current division between the effective external resistance shunting the base lead and the resistance seen looking into the base of a transistor (generator resistance). Another limitation in the transistor amplifier is because of the built-in limitations in the input signal conditions. That is the transistor cannot accept large amplitudes of signal. If the base signal current is increased enormously, the collector will saturate. This will produce severe distortion at the output signal of the transistor amplifier in the form of clipping.

Objective

To study the effects of base-emitter circuitry on the gain of the transistor amplifier.

Experimental Set Up

Equipments needed

1. CRO—1 No.
2. Power supply 30V/1A—1 No.
3. Audio oscillator—1 No.

Components required

1. Transistor CIL 531 or equivalent—1 No.

2. Resistor 470 ohms 10% $\frac{1}{4}$ W—1 No.
3. Resistor 3.9 kilo ohms 10% $\frac{1}{4}$ W—1 No.
4. Resistor 4.7 kilo ohms 10% $\frac{1}{4}$ W—1 No.
5. Resistor 33 kilo ohms 10% $\frac{1}{4}$ W—1 No.
6. Resistor 100 kilo ohms 10% $\frac{1}{4}$ W—1 No.
7. Resistor 1 mega ohm 10% $\frac{1}{4}$ W—1 No.
8. Capacitor (polyster or mica) 0.1 mfd.—1 No.
9. Capacitor (electrolytic) 15V,10 mfd.—1 No.

Procedure

Rig up the circuit as shown in Fig. 19.1. Keep the supply voltage as 15 volts and note the quiescent voltage conditions at the collector, base and emitter. Connect the audio oscillator and keep the signal frequency at, say, 2 kHz. Vary the audio oscillator output such that the voltage across the 100 kilo ohms

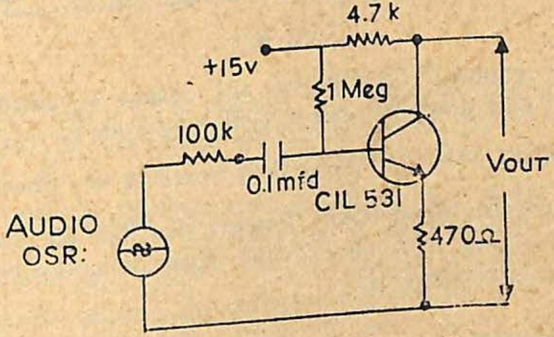


Fig. 19.1

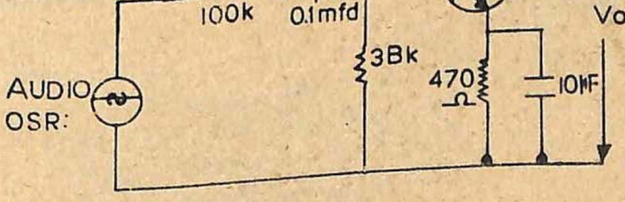


Fig. 19.2

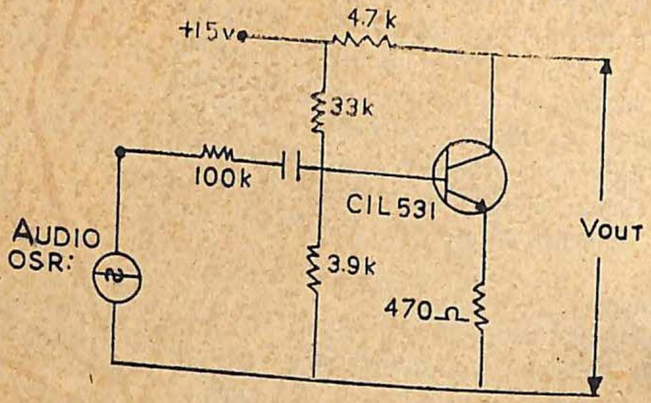


Fig. 19.3

resistor is around 1 volt. Observe the output waveform in the CRO and note down its peak to peak amplitude for a good sine-wave. Calculate the gain using the formula $A = \frac{V_o}{V_i}$. Repeat the experiment for different frequencies. Rig up the circuits as shown in Fig. 19.2 and 19.3 and repeat the above experiment and tabulate the readings.

Review Questions

1. From the data, find out the current gain for each of the three circuits.
2. Calculate the approximate value of the voltage gain for each of the circuit from the transistor parameter and values of the circuit components.
3. What are the differences in the performance of the three circuits ?
4. What is the maximum input voltage which can be applied to the circuit shown in Fig. 19.3 for a distortion-free output?

20

FORWARD CURRENT TRANSFER RATIO OF A TRANSISTOR

Theory

Forward current transfer ratio of a transistor in the common emitter mode of connection can be defined as the ratio of the collector current to the base current. When direct currents are considered, this dc forward current transfer ratio is denoted by h_{FE}. When small signal currents are considered, the forward current transfer ratio, under this condition is not same as h_{FE}. For a particular value of dc collector current, the ratio of the signal collector current to the signal base current, when the signal collector to base voltage is set to zero, is defined as ac current transfer ratio h_{fe}. The forward current transfer ratio is dependent on many factors like the frequency of the signal current and the value of dc collector current.

Objective

To determine the common-emitter short circuit current gain of a transistor and note its variations with changes in frequency and dc collector current.

Experimental Set Up

Equipments needed

1. Signal generator—1 No.
2. Power supply 30V/1A—1 No.
3. VTVM—2 Nos.
4. Milliammeter 0-50 ma—1 No.

Components required

1. Transistor CIL 531 or equivalent--1 No.
2. Resistor 1 k. ohm 10% $\frac{1}{4}$ W—2 Nos.
3. Resistor 3 k. ohms 10% $\frac{1}{4}$ W—1 No.
4. Potentiometer (linear) 25 k. ohms--1 No.
5. Inductor 100 mH, 25 ma—1 No.
6. Capacitor (Electrolytic) 10 mfd/15V—1 No.

Procedure

Rig up the circuit as shown in Fig. 20.1. Keep the potentiometer to its maximum resistance position. With the supply voltage set to + 15V, switch on the power supply. Adjust the potentiometer so that a dc collector current of, say, 4 ma flows. Set the oscillator at frequency of 500 Hz and adjust the amplitude of the output of the oscillator so that the base circuit VTVM reads 0.2 volt rms. This indicates that the base signal current flowing through the circuit will be around 66 ma. Now read the voltage in the collector circuit VTVM and calculate the collector current dividing this by the collector resistance. Compute the current transfer ratio h_{fe}. Vary the frequency, keeping the amplitude of the oscillator in steps of 500 Hz. Enter the readings in a tabular form. Beyond 5 kHz, the step of the frequency may be increased to 5 kHz.

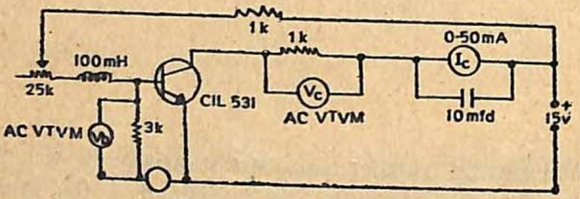


Fig. 20.1

Set the oscillator to a frequency of 500 Hz and reduce the dc collector current to its minimum value by adjusting the potentiometer and, if necessary, by reducing the supply voltage. Maintaining the base circuit VTVM reading at 0.2 V, read the collector circuit VTVM for increasing value of dc collector current and tabulate these readings. compute h_{FE} for different values of dc collector current.

Review Questions

1. In what way does h_{fe} vary with collector current ? Do you find h_{fe} fairly constant over any range of collector current?
2. Can a low distortion small gain amplifier be designed using this transistor ?
3. Discuss the reasons for the reduction of h_{fe} with increasing frequency and collector current.

21

LOW FREQUENCY RESPONSE OF A TRANSISTOR AMPLIFIER

Theory

In the amplifier circuits, capacitors are used to bypass resistors and for coupling signal currents to the exclusion of direct current. The values of the capacitors should be such that their reactances should be low even at low frequencies. The practical size limits the use of high value of capacitors in the circuits. Because of this, there is a limitation to the low frequency response of a transistor amplifier.

Objective

To determine the low frequency response of the transistor amplifier caused by various circuit elements.

Experimental Set Up

Equipments needed

1. Audio oscillator—1 No.
2. Power supply 30V/1A—1 No.
3. VTVM—1 No.

Components required

1. Transistor CIL 531 or equivalent—1 No.
2. Resistor 1.2 k. ohms 10% ¼ W—1 No.
3. Resistor 2.2 k. ohms 10% ¼ W—1 No.
4. Resistor 4.7 k. ohms 10% ¼ W—1 No.
5. Resistor 5.6 k. ohms 10% ¼ W—1 No.
6. Resistor 27 k. ohms 10% ¼ W—2 Nos.
7. Capacitor (Electrolytic) 150 mfd/15 V—1 No.

8. Capacitor (electrolytic) 10 mfd/15 V—1 No.
9. Capacitor (mica or polyster) 0.01 mfd—1 No.
10. Capacitor (mica or polyster) 0.02 mfd.—1 No.

Procedure .

Rig up the circuit as shown in Fig. 21.1 with C_c shorted and keeping the value of C_e as 150 mfd, R_s as 27 k. ohms. Set the oscillator output as 0.5 V at frequency of 1 kHz. If a CRO is available, see the output waveform and confirm that the waveform of the output is without any distortion. Keeping the output of the oscillator constant, note the output of the amplifier in the VTVM for frequencies from 1 kHz to, say, 10 Hz in suitable steps. Tabulate the readings. Repeat the experiment for $C_e = 10$ mfd.

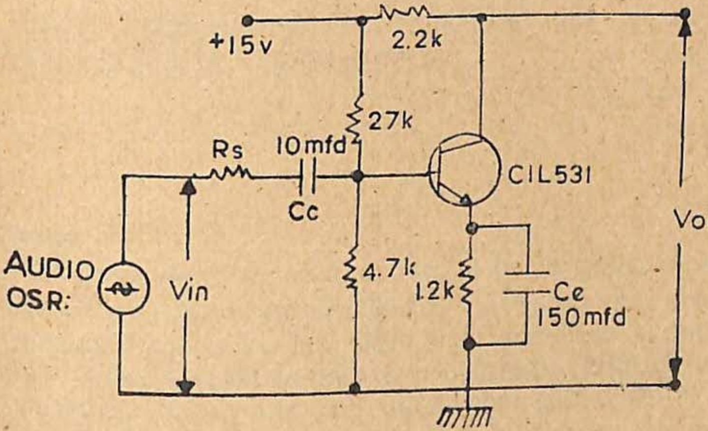


Fig. 21.1

Modify the circuit with Cc connected for 0.02 mfd, $R_s = 27$ k. ohms and $C_e = 150$ mfd. Conduct the experiment as explained above. Repeat the experiment by changing C_c with 0.01 mfd condenser. To study the response of source resistance, change the value of R_s to 5.6 k. ohms, C_c to 0.02 mfd and C_e to 150 mfd. Repeat the experiment. Plot the response curves in all the cases.

Review Questions

1. Find out the −3dB point from the curves in all the cases and compare.

2. Calculate the mid-band gain of the circuit for a source resistance of 27 k. ohms, taking other parameters from the data sheet for the transistor.
3. Discuss the effects of the source resistance and coupling capacitor values on the low frequency response of the circuit.

22

HIGH FREQUENCY RESPONSE OF A TRANSISTOR AMPLIFIER

Theory

Generally when a transistor is used as an amplifier, the upper frequency response of the amplifier does not come up to the high frequency response of the single transistor given in the data sheet. This is because of the external circuitry incorporated in the amplifier circuit and also due to the 'miller effect'. The upper frequency limit will be lower than the beta cut-off frequency of the transistor used. Any capacitance present between collector and base of the transistor is detrimental in the high frequency gain because this capacitance reflected as a much larger equivalant capacitance appearing in parallel with input signal. This reflected capacitance offers a low resistance path to the high frequency signal applied to the base.

Objective

To study the effect of external circuitry on the high frequency response of the common-emitter amplifier.

Experimental Set Up

Equipments needed

1. Audio oscillator—1 No.
2. Power supply 30V/1 A--1 No.
3. VTVM (having good frequency response)— 1 No.

Components required

1. Transistor SA 188 or equivalent—1 No.
2. Resistor 1.2 k. ohms 10% ¼ W—1 No.

3. Resistor 2.2 k. ohms 10% $\frac{1}{4}$ W—1 No.
4. Resistor 4.7 k. ohms 10% $\frac{1}{4}$ W—2 Nos.
5. Resistor 33 k. ohms 10% $\frac{1}{4}$ W—1 No.
6. Resistor 47 k. ohms 10% $\frac{1}{4}$ W—1 No.
7. Resistor 100 k. ohms 10% $\frac{1}{4}$ W—1 No.
8. Capacitor (electrolytic) 25 mfd/15 V—1 No.
9. Capacitor (mica or polyster) 0.05 mfd—1 No.
10. Capacitor (mica or polyster) 100 pfd—1 No.

Procedure

Rig up the circuit with R_L as 2.2 k. ohms and R_2 as 47 k. ohms and C_{cb} removed as shown in Fig. 22.1. Set the supply voltage to − 15 V and switch on the circuit. See if the circuit is operating properly by measuring the V_{ce} drop. The transistor should neither be in the cut-off nor in the saturation region. Adjust the oscillator output to be 0.5 V and measure the same with VTVM. Starting from a frequencey of 1 kHz and keeping the input amplitude constant, measure the output using the VTVM in steps of 10 kHz. Make a tabular column showing the frequency and output parameters for a constant input.

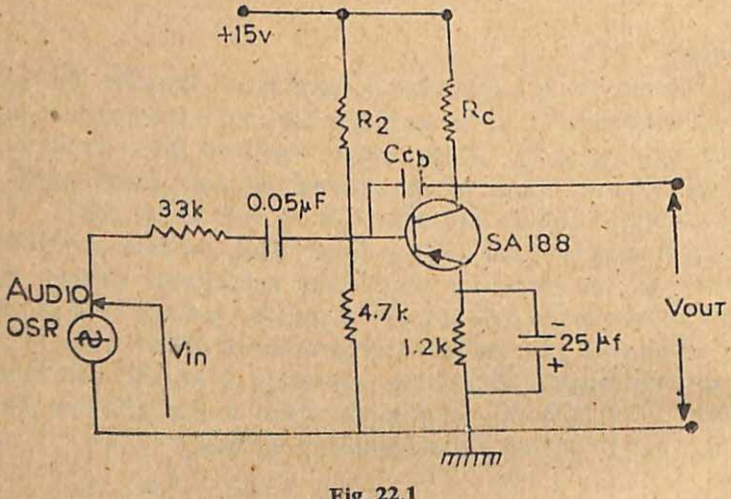


Fig. 22.1

Add a 100 pfd in the place of C_{cb} and repeat the experiment as explained above. This experiment will give the effect of increased collector-base capacitance in the circuit.

To study the effect of increased load resistance, disconnect C_{cb} and increase the load resistor to 4.7 k. ohms. Simultaneously change R_2 to 100 k. ohms to prevent the transistor becoming saturated. Obtain the data of frequency and output for a constant input condition and tabulate. Draw the graph for all the three conditions and compare the frequency responses.

Review Questions

1. From the graph determine the -3 dB points.
2. Calculate theoretically the upper 3 dB points taking the relevant data for the transistor from the data sheet.
3. Explain the differences, if any, between theoretical and experimental upper -3 dB points.
4. What role does the parameter h_{ie} play in determining the upper frequency limit of a transistor amplifier ?

23

TRANSFORMER COUPLED POWER AMPLIFIER

Theory

Any amplifier driven by large input signals to produce sufficiently large power to the load is generally called a power amplifier. The signal current and voltage swing vary widely about a quiescent point. This means that the transistor cannot be represented accurately by its fixed values of its parameters. This is because, under large signal conditions, the current amplification factor for example is not a fixed value. When the object is to deliver large amounts of power to the load, a R-C type of coupling used in small signal amplifiers becomes very inefficient. Hence, a transformer coupling with all its attended limitations on frequency is the optimum choice for power amplification. The efficiency of the transformer coupled amplifier is quite high and this varies with the type of amplifier like such as class A, class B, etc.

Objective

To investigate the properties of a transformer coupled power amplifier under class A and class B modes of operation and to find the efficiency of the amplifier.

Experimental Set Up

Equipments needed

1. Audio oscillator—1 No.
2. Power supply 30V/1A—1 No.
3. CRO—1 No.

4. VTVM—1 No.

Components required

1. Transformer with a suitable frequency response of, say, 5kHz—1 No.
2. Output transformer 10 : 1—1 No.
3. Transistor 2 N 3055 or equivalent—1 No.
4. Resistor 10 ohms 10% 1 W—1 No.
5. Resistor 100 ohms 10% ½ W—1 No.
6. Resistor 100 ohms 10% 1 W—1 No.
7. Resistor 5 ohms 10% 10 W—1 No.

Procedure

Wire the circuit as shown in Fig. 23.1. Connect dc voltmeter (VTVM) across the emitter resistor R_e and turn on the dc supply and raise its value to 15 V. The emitter voltage should increase from 0.5 V to 0.7 V. If the initial voltage indicates an emitter current of value in excess of 0.4 A, the resistor R_b may be increased to bring the emitter current to 0.7 A. After the transistor has warmed up, note the value of the emitter voltage.

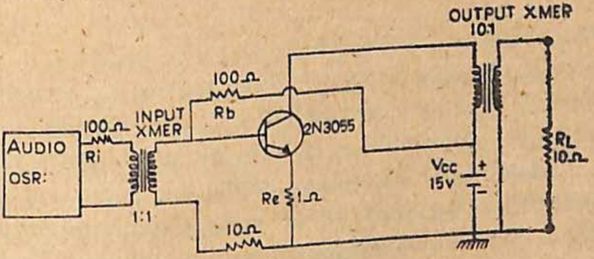


Fig. 23.1

Operation as a Class A Amplifier

Connect the vertical amplifier of a CRO to the output of the amplifier. Switch on the audio oscillator and keep the frequency at, say, 500 Hz position and the amplitude at about $2V_{pp}$. See the waveform in the CRO. If the waveform is distorted, reduce the amplitude of the signal source until a good sinewave is displayed on the CRO. With the VTVM in ac position measure the voltage input to the primary of the input transformer and the output voltage across the load. Term them as V_{in} and V_{out}. Measure the currents flowing in the resistor R_i by opening the resistor and introducing the VTVM in the current mode. Similarly measure the base current i_b, emitter current i_e and the output current i_o. Calculate the input and output power. Vary the frequency and record the output power and plot a graph between frequency and output.

$P_{in} = V_{in} \times$ current through R_i

$P_{out} = V_{out} \times i_o$

$$\text{Power amplification factor} = \frac{P_{out}}{P_{in}}$$

Connect in VTVM in the dc mode and measure the current from the power supply, say, I_D.

Power consumed $= V_{CC} \times I_D$

$$\text{Percentage efficiency} = \frac{P_{out} \times 100}{V_{CC} \times I_D}$$

Operation as a Class B Amplifier

Remove the biasing resistor R_b from the circuit. Switch on the power supply. Keep the voltage at 15 V. Observe the waveform at the output of the amplifier, at the emitter of the circuit and at the base. Sketch these waveforms. With the audio oscillator in the off condition, measure the dc voltage at the emitter. Connect the CRO at the output and switch on the oscillator. Increase the amplitude so that the output has only a positive half of the waveform. Repeat the measurements of current and voltage as explained for class A operation. Repeat the experiment for different frequencies and plot a graph between frequency and output. Calculate the power amplification factor and efficiency.

Review Questions

1. How the heat generated in the transistor can be removed? Is it any important problem to think of cooling system for the power stage in the design?
2. What is the effect on the quiescent current, output voltage waveform and base voltage waveform on account of the removal of the biasing resistor R_b?
3. Is it sufficient to use a single ended class B power amplifier stage for amplification of audio signals?

24

PUSH-PULL TRANSFORMERLESS CLASS B POWER AMPLIFIER

Theory

Class B amplifiers use low bias currents and hence reduce the amount of collector junction heating In class B operation the current flow in the collector lead of the transistor is for one half of the cycle only. Two transistors are therefore required to be wired in a push-pull circuit to obtain the complete waveform. The output transformerless bridge type circuit chosen for this experiment is a very flexible arrangement for power amplification.

Objective

To study the operation and requirements of the bridge type push-pull class B transistor amplifier.

Experimental Set Up

Equipments needed

1. Power supply 30V/1A—1 No.
2. Audio oscillator—1 No.
3. VTVM—2 Nos.
4. CRO—1 No.

Components required

1. Transistor SL 100 or 2N 697—2 Nos.
2. Transformer with capability of 1.3 V and 5 V for an input of 2V—1 No.
3. Resistor 1 ohm 10% 2W—2 Nos.
4. Resistor 10 ohms 10% 2W—1 No.

5. Resistor 1 k. ohm 10% $\frac{1}{2}$ W—2 Nos.
6. Resistor 1.2 k. ohms 10% $\frac{1}{2}$ W—1 No.
7. Resistor 10 k. ohms 10% $\frac{1}{2}$ W—1 No.
8. Capacitor (electrolytic) 100 mfd/20V—1 No.

Procedure

Wire the circuit as shown in Fig. 24.1. With audio oscillator off, measure the dc voltages at the emitter of T_2, V_{CE} of T_1 and T_2. In order to ensure that the input transformer will supply 2 signals 180° phase opposition to the transistor bases, following procedure may be followed.

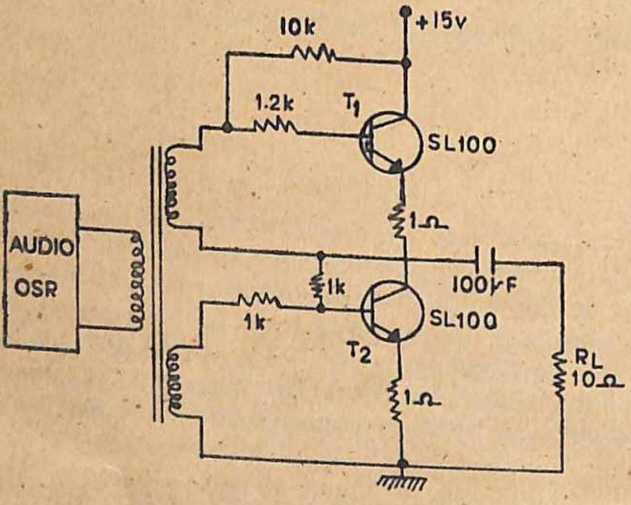


Fig. 24.1

Wire the 6.3 V and 5 V windings of the transformer in series. Measure the voltage across the series combination by applying a 2 V input from the audio oscillator. If the windings are correctly phased, then, the output should be only 1.3 V. Otherwise, it will be 11.3 V and one of the windings should be reversed to correct the phase. Connect this corrected phase position of the transformer to the transistor bases. Set the output frequency of the oscillator at about 1 kHz, switch on the power supply and observe the output waveform in the CRO.

With the CRO connected as above, increase the signal level of the oscillator till distortion appears in the waveform. Stop the increase at this point and note the peak to peak value of the output voltage. Using a VTVM measure the current flowing through R_L, calculate the power. Repeat the experiment for different frequencies up to 5 kHz. Switch off the supply and the oscillator and reverse the phase of the windings. With the input of 1 V rms supply from the oscillator, observe the waveform.

Review Questions

1. Calculate the maximum undistorted output power.
2. Calculate the quiescent collector dissipation for each transistor.
3. Increase the voltage, say, 20 V and calculate the possible power output.
4. Can the emitter resistors be bypassed ? If not. why ?
5. Sketch the waveforms of the output for the normal operation and incorrect phase operation.

25

OPERATIONAL AMPLIFIER

Theory

Operational amplifiers have got very high open-loop gain of 80 dB and above, high input impedance and low output impedance. They are widely used in analog computers for summing activity. This is a versatile type of amplifier because by using suitable feedback circuits the characteristics of the amplifier can be controlled and can be put to a wide variety of uses. A triangular symbol is used to represent the entire amplifier. In modifying the amplifier using negative feedback network, care should be taken to see that the feedback circuit is connected at the inverting input. The signal can be applied to any of the input terminals depending upon the required input impedance of the amplifier. When the signal is applied to the non-inverting input of the amplifier, input impedance becomes very high at both the input terminals, because the feedback voltage is nearly equal to input voltage and the two voltages appear as common-mode input signal. Referring to Fig. 25.1, it is possible to calculate β, the feedback ratio as $\frac{R_1}{R_1+R_f}$. The gain of the amplifier therefore is reduced and the gain $K_f = \frac{1}{\beta} = \frac{R_1+R_f}{R_1}$, where $K_f\beta \gg 1$.

The amplifier gain increases when the feedback resistance is connected in the inverting terminal. Figure 25.2 shows the connections given in this way. The non-inverting input terminal is maintained at signal ground potential by capacitor C. The amplifier input current i_a is very small compared to i_1 and i_f.

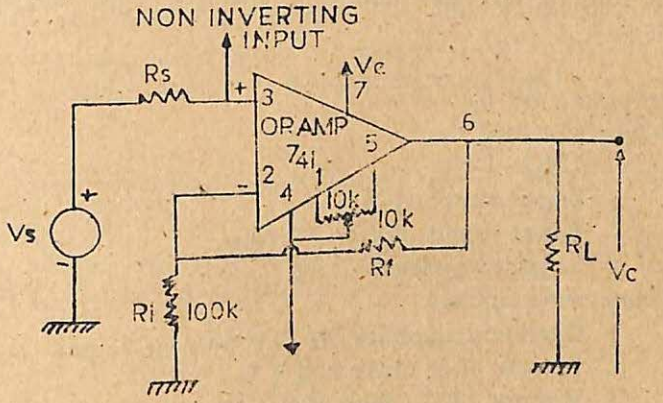


Fig. 25.1

Therefore at the inverting node the current equation can be written as $i_1 = i_f$. The input voltage is also very small at the inverting terminal of the amplifier. This voltage at this terminal is the output divided by the amplifier gain. This value will also be very small. Because of this low voltage at this point this level can be assumed to be zero on comparing with the output voltage and driving point voltage. This point is called the virtual ground. Writing the equation for current we get,

$$i_1 = \frac{V_s}{R_s + R_1}$$

$$i_f = \frac{V_0}{R_f}$$

Since $$i_1 = i_f$$

$$\frac{V_s}{R_s + R_1} = \frac{V_0}{R_f}$$

$$\frac{V_s}{V_o} = \frac{R_s + R_1}{R_f}$$

The closed loop voltage gain $K = \frac{V_0}{V_s} = \frac{R_f}{R_s + R_1}$

If the input voltage of the amplifier is considered as V_i and the value of R_1 is much higher than the source impedance of the generator, then, the voltage gain $K' = \frac{V_0}{V_i} = \frac{R_f}{R_1}$.

Objective

To study the amplifier gain characteristics of the operational amplifier.

Experimental Set Up

Equipments needed

1. CRO—1 No.
2. Signal source—1 No.
3. Power supply 30V/1A—2 Nos.
4. dc microammeter—1 No.

Components required

1. Operation amplifier 741 or equivalent—1 No.
2. Resistor 10 k. ohms 10% $\frac{1}{4}$ W—2 Nos.
3. Resistor 100 k. ohms 10% $\frac{1}{4}$ W—2 Nos.
4. Resistor 680 k. ohms 10% $\frac{1}{4}$ W–1 No.

Procedure .

Rig up the circuit as shown in Fig. 25.1. Set the power supply voltages of both positive and negative exactly at 10 volts. Feed a sinusoidal signal of amplitude 1 volt at, say, 500 Hz. See the output in a CRO. Vary the input frequency keeping the amplitude of the signal constant. Note the frequency response of the amplifier. Connect a dc microammeter between the signal source and the input terminal and measure the input current for an input dc voltage of 1 V.

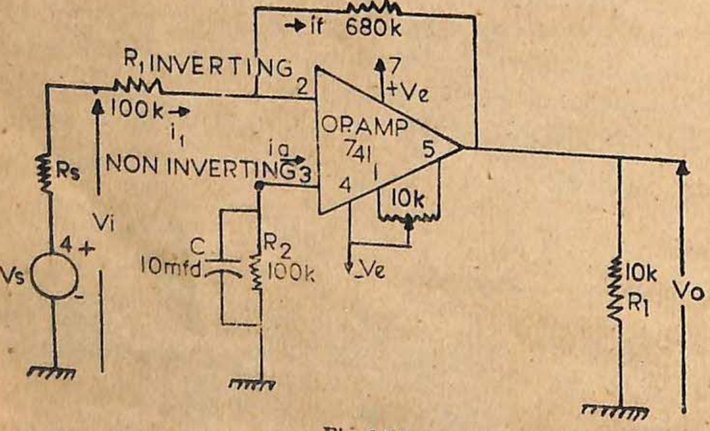


Fig. 25.2

Rewire the circuit as shown in Fig. 25.2. Feed a signal of amplitude of 5 mV at the input and note the amplitude of the waveform on the CRO at the output. Vary the frequency and study the frequency response of the amplifier. Vary the ratio of R_f and R_1 for higher gains and repeat the experiment.

Review Questions

1. Discuss the gain-bandwidth aspects of the operational amplifier.
2. How the operational amplifier is superior to a conventional type of high gain amplifier ?

26

OPERATIONAL AMPLIFIER—AS SUMMING AMPLIFIER

Theory

One of the uses to which the operational amplifier is often put to is in the summing of voltages. Writing the current equation at the input node, it is possible to write down the relation for Fig. 26.1 in the following manner:

$$i_1+i_2+i_3+i_4 = i_f \tag{1}$$

But $i_1 = \frac{V_1}{R_1}$, where V_1 is the input voltage. (The input point acts as a virtual ground.)

$$i_2 = \frac{V_2}{R_2},\ i_3 = \frac{V_3}{R_3},\ i_4 = \frac{V_4}{R_4} \text{ and } i_f = \frac{V_0}{R_f}$$

Therefore $$\frac{V_0}{R_f} = \frac{V_1}{R_1}+\frac{V_2}{R_2}+\frac{V_3}{R_3}+\frac{V_4}{R_4}+\ldots\ldots \tag{2}$$

$$V_0 = \frac{R_f}{R_1}V_1+\frac{R_f}{R_2}V_2+\frac{R_f}{R_3}V_3+\frac{R_f}{R_4}\,V_4\ldots\ldots \tag{3}$$

Any number of inputs can be used for summation. In case a single addition is required then all the values of resistors R_1, R_2, R_3 and R_4 can be made equal to R_f and the equation (3) can be modified as $V_0 = V_1+V_2+V_3+V_4\ldots\ldots$ (4)

Objective

To study the summing operation of the operational amplifier.

Experimental Set Up

Equipments needed

1. CRO—1 No.

2. Power supply 30V/1A—2 Nos.
3. Voltage sources—As many desired as the number of inputs.

Components required

1. Operational amplifier 741 or equivalent—1 No.
2. Resistor 2.7 k. ohms 10% ¼ W—1 No.
3. Resistor 10 k. ohms 10% ¼ W—5 Nos.
4. Capacitor (electrolytic) 1 mfd/20V—1 No.
5. Potentiometer 10 k. ohms (wire wound)—1 No.

Procedure

Rig up the circuit as shown in Fig. 26.1. Set the voltages of the power supplies to +10 and −10 volts. Care should be taken for proper grounding. Connect the power supplies to the amplifier. With all the inputs grounded, see the output for any offset voltage. Adjust the potentiometer for reducing the offset to zero. Then feed the input voltage from the voltage sources to the respective input points so that the input at any one point does not exceed 0.5 volt. See the output waveform. Vary the frequency of the source and note the output amplitude.

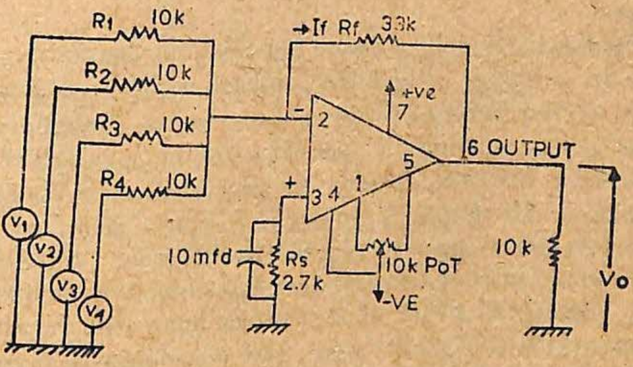


Fig. 26.1

Review Questions

1. Discuss the frequency limitation of the summing amplifier.
2. What is the maximum number of inputs that can be given to a summing amplifier ?

27

PHASE SHIFT RC OSCILLATOR

Theory

Feedback offers a very good possibility to convert an amplifier into an oscillator. When the feedback becomes positive, the $A\beta$ term (gain × feedback ratio) exceeds unity, oscillations set in. This is an undesirable phenomenon in an amplifier circuit. Whenever a waveform is to be generated, as in the case of an oscillator, the feedback comes in handy. There are different methods and circuit arrangements available for feedback oscillators. In a transistor circuit the common emitter orientation offers 180 degrees of phase shift between input and output. If this output is fed back to the input, with an additional phase shift of 180 degrees, using a transformer for instance, the input has the same phase as the output and causes sustained oscillations.

An RC network can be designed to provide the additional phase shift between the output and input for the common emitter transistor configuration. The circuit shown in the Fig. 27.1 reveals that the transistor output point is connected through a three stage phase shift network. Each RC pair provides a phase shift of 60 degrees. The loop gain at a particular frequency is greater than unity, oscillations will build up. These oscillations will reach a steady state because of the nonlinear relation between the gain and the signal amplitude. The phase shift network of the circuit works as a high-pass filter. Low frequencies are blocked by the capacitor so that loop gain is low. High frequencies easily pass through the capacitors. At the high frequencies the phase shift experienced is not sufficient to sustain the oscillations. Only at one frequency, the necessary and sufficient conditions, the loop gain and phase shift will be fulfilled and oscillations sustained. A complete ac equivalent circuit of the Fig. 27.1 is shown in Fig. 27.2.

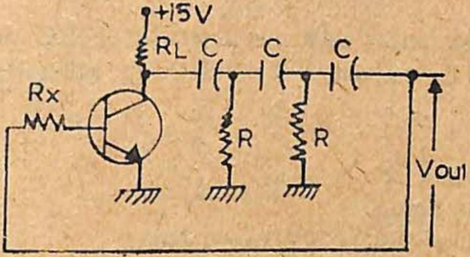


Fig. 27.1

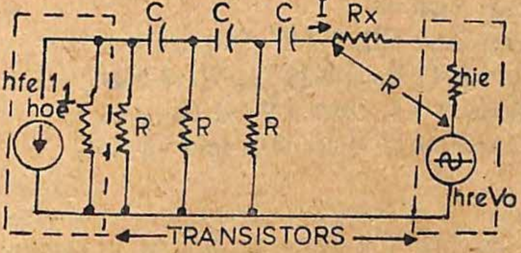


Fig. 27.2 (a)

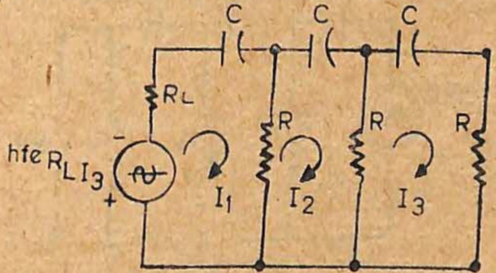


Fig. 27.2 (b)

Writing the loop equations and comparing the real and imaginary parts, it can be shown that $w^2 = \frac{1}{C^2[4RR_L+6R^2]}$ and $h_{fe} = 23 + \frac{29R}{R_L} + \frac{4R_L}{R}$ where R is the resistance of the phase shift network and R_L is the load resistance. For a value of $C = 0.01$ mfd, $R_L = 5$ k. ohms and $R = 1$ k. ohm, the frequency of oscillation is around 6 kHz and the h_{fe} of the transistor required is a minimum of 49.

Objective

To study the phase shift characterstics of RC network and use the same in a phase shift oscillator for generating a sinusoidal output.

Experimental Set Up

Equipments needed
1. Power supply 30V/1A—1 No.
2. Oscillator—1 No.
3. Double beam CRO—1 No.

Components required
1. Transistor CIL 532 or equivalent—1 No.
2. Resistor 1 k. ohm 10% $\frac{1}{4}$ W—3 Nos.
3. Resistor 5 k. ohms $\frac{1}{4}$ W—1 No.
4. Capacitor (Polyster) 0.01 mfd—3 Nos.

Procedure

Connect the circuit as shown in Fig. 27.3. Feed a signal of 6 kHz to the input and monitor the output and compare the waveforms using a double beam oscilloscope and calculate the phase shift. Vary the frequency and study the characterstics. Rig up the circuit as shown in Fig. 27.4 and find out the amplitude and frequency of the output waveform. If a distortion analyser is available, measure the output distortion and compare the distortion with the waveform obtained in the CRO. Change the

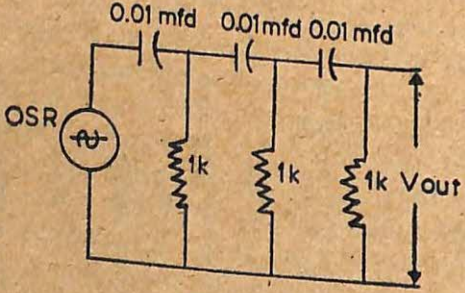


Fig. 27.3

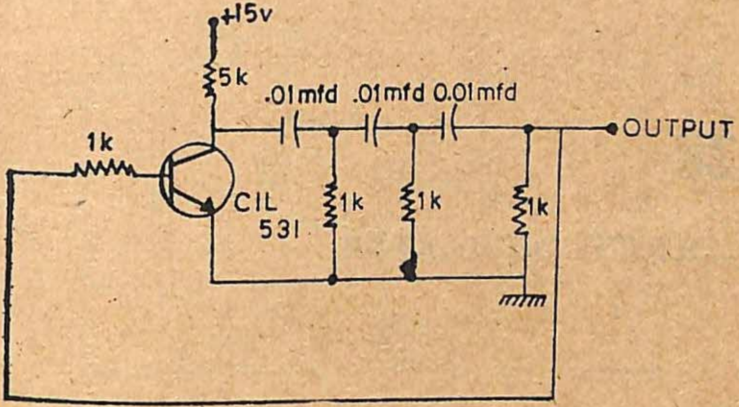


Fig. 27.4

values of *R* and *C* suitably for a 10 kHz and 15 kHz oscillations and repeat the experiment.

Review Questions

1. With vector diagram discuss the phase shift introduced by a capacitor for any signal input.
2. Derive the relationship to obtain oscillation in a phase shift oscillator.

28

COLPITTS OSCILLATOR

Theory

In the family of oscillators, colpitts oscillator using inductor and capacitors is a widely used circuit for reasons of stability of oscillation. In the colpitts oscillator the feedback is provided from the junction of the split load capacitors to the base of the transistor. When the feedback is sufficiently positive, the circuit goes into oscillation. There can be three different configurations for this type of oscillator, viz., common-base, common-emitter and common-collector. This type of circuit requires minimum number of components only. Figure 28.1 shows a typical oscillator connected in the common-emitter configuration.

Figure 28.2 gives the equivalent circuit for analysis. Writing the loop equations and simplifying them and equating the imaginary portion of the circuit determinant to zero we get the expression for angular frequency of oscillation

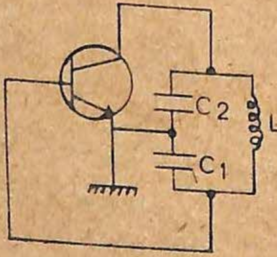


Fig. 28.1

$$w^2 = \frac{h_{oe}}{C_1 C_2 h_{ie}} + \frac{1}{LC_1} + \frac{1}{LC_2} \qquad (1)$$

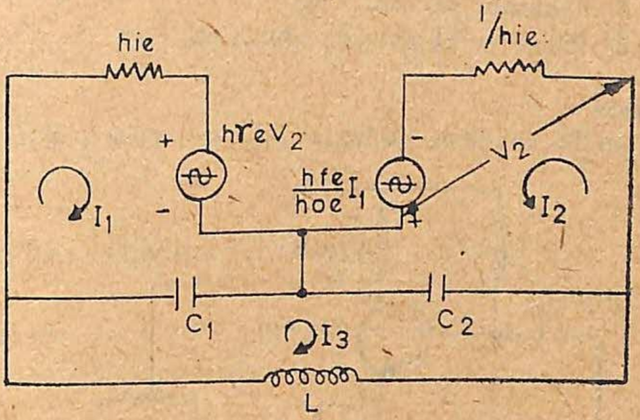


Fig. 28.2

For practical values of the parameters, the oscillator angular frequency,

$$w^2 = \frac{C_1+C_2}{L(C_1+C_2)} \tag{2}$$

This expression represents the resonant frequency of a tank circuit with L paralleling a series branch of C_1 and C_2. Equating the real part of the determinant we get,

$$\frac{h_{fe}}{\Delta he} = \frac{C_1}{C_2} \tag{3}$$

where $$\Delta he = h_{ie} \times h_{oe} - h_{re} \times h_{fe} \tag{4}$$

Objective

To study the characteristics of a colpitts oscillator.

Experimental Set Up

Equipments needed

1. Power supply 30V/1A—1 No.
2. CRO—1 No.
3. Frequency counter—1 No.

Components required

1. Transistor CIL 531 or equivalent—1 No.
2. Resistor, 470 ohms, 4, 7, 18, 47 k. ohms 5% ¼ W—1 No. each
3. Inductor 5 mh—1 No.
4. Capacitor 0.047 mfd—1 No.

5. Capacitor 500 pfd—1 No.
6. Capacitor 0.1 and 0.01 mfd—1 No. each

Procedure

Rig up the circuit as shown in Fig. 28.3. Give a +15 volts supply. See the waveform in the CRO, across the tank circuit. Measure the amplitude and frequency. Vary the supply voltage slightly and observe the variation in the output.

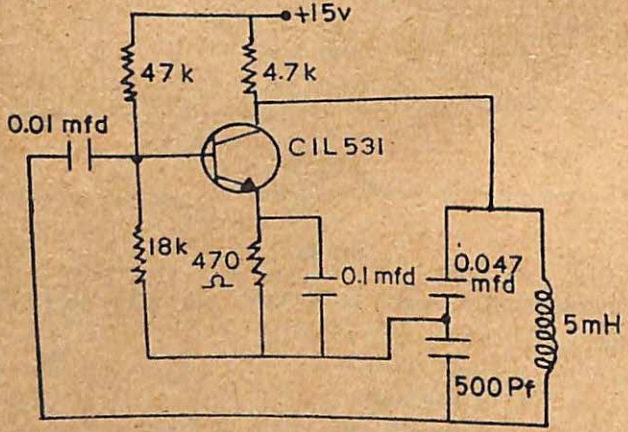


Fig. 28.3

Review Questions

1. Discuss the condition for oscillation.
2. What is the advantage of LC oscillator with reference to colpitts oscillator ?
3. How does aging of transistor affect the oscillation ?

29

CRYSTAL OSCILLATOR

Theory

Stable fixed frequency oscillator can be designed using a quartz crystal in the place of conventional *L* and *C*. This is because the equivalent circuit of the quartz crystal approximates an L.C. circuit with a very high quality factor *Q*. For good stability of oscillation **GT cut** crystalls are used. A typical oscillator circuit is shown in Fig. 29.1. Crystals of different frequencies are available in the market. Depending upon the requirements a suitable crystal can be chosen. The transistor used in the circuit should also have the frequency capabilities to give sustained oscillations. Crystal oscillators are widely used in the **DVMs** and digi-

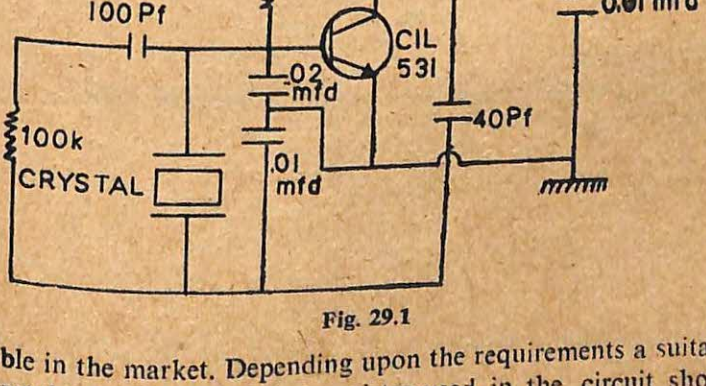


Fig. 29.1

tal frequency counters. High degree of stability in oscillation can be achieved using oven controlled crystals.

Objective

To study the crystal oscillator circuit.

Experimental Set Up

Equipments needed

1. Power supply 30V/1A—1 No.
2. CRO—1 No.

Components required

1. Trasnsistor 2N 2369 or equivalent—1 No.
2. Crystal 100 KHz—1 No.
3. RF choke 6 mh--1 No.
4. Resistor 150 ohms, 22 k. ohms and 100 k. ohms 10% ¼ W—1 No. each
5. Capacitor 40 pfd, 100 pfd 350 pfd, and 0.02 mfd (polyster)—1 No. each
6. Capacitor 0.01 mfd (polyster)—2 Nos.

Procedure

Rig up the circuit as shown in Fig. 29.1. Keep the supply voltage at +15V and switch on the power supply. See the waveform in an oscilloscope. Determine the amplitude of the oscillation. Calculate the frequency of oscillation from the waveform displayed in the CRO.

Review Question

Discuss the frequency stabilisation techniques used in the oscillator circuits.

30

BISTABLE MULTIVIBRATOR

Theory

The bistable multivibrator circuit with many variations find wide applications in digital circuitry like digital computers. Bistable multivibrator is known by many names : binary, flip-flop, scale-of-two, divided-by-two, and Eccles Jordan. Basically the flip-flop is an overdriven amplifier connected in the manner as shown in Fig. 30.1. A_1 and A_2 are shown as two amplifiers.

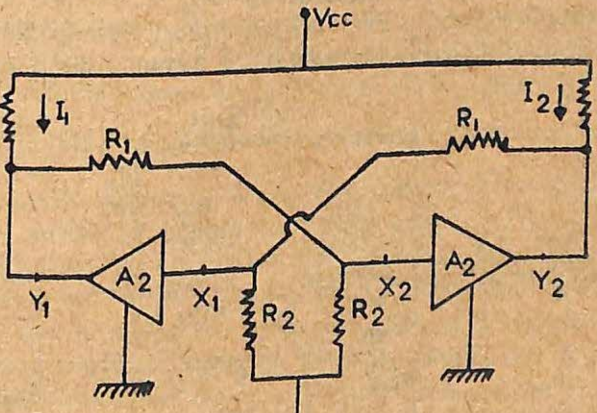


Fig. 30.1

Because of the symmetry of the circuit the quiescent current in each of the amplifiers are the same, *i.e.*, $I_1 = I_2$. This extreme case is possible when the devices are identical in all respects. The practical consideration is that there should be minute fluctuations in the current in one of the amplifiers. If I_1 increases, this voltage at the output Y_1 will decrease. This in turn decreases the input voltage at X_2. This change in voltage at X_2 will be amplified and inverted by A_2 and fed to X_1. The voltage at X_1 becomes more positive and this causes an increase in current I_1. This cycle of events repeat itself. The current I_1 continues to increase while that I_2 continues to decrease. The circuit progressively moves away from the initial condition. All this is due to regenerating feedback shown in the circuit and this will occur only when the loop gain of the circuit is larger than, unity. The device which is *on* goes to saturation and the other goes to cut-off. At this stage both the conditions are stable and the circuit remains in the stable state unless external triggering is brought out change the state. Due to changes in temperature and aging of components, the parameters of the device vary widely and will cause appreciable changes in the quiescent point. In some cases a larger drift will cause the device which is in the operating region to be driven to cut-off condition. In such a case both the devices in the binary are below cut-off and the circuit become useless. Flip-flop circuits are constructed with components tolerances of the order of 10%.

The circuit shown in Fig. 30.2 is a typical flip-flop. This output from T_1 is coupled to the base of T_2 through the resistance

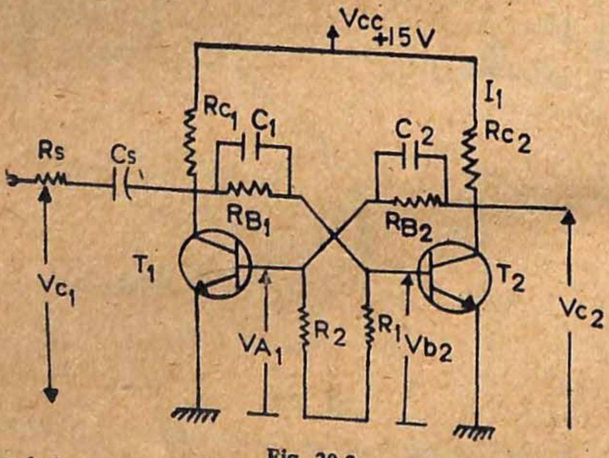


Fig. 30.2

R_{B_2} and the output of T_2 is coupled to the base of T_1 through the resistanc R_{B_1}. Initially assume that the current flowing through T_1 is slightly more than that through T_2. This causes a fall in voltage at the collector of T_1 which is transferred to the base of T_2. This negative voltage drives T_2 to cut-off, raising the collector voltage of T_2 towards V_{CC}. This voltage is fed to the base of T_1 through R_{B_1} causing T_1 to go to saturation. Thus T_1 goes to saturation and T_2 to cut-off. These two states will be preserved until a negative pulse fed to the base T_1 to drive it to cut-off. Then this change of state in T_1 will cause an equal change in the state of T_2. That is T_2 will be *on* and T_1 will be in cut-off state. These two states will be stable until another negative pulse is fed to the base of T_2.

The design of a flip-flop is carried out in the following manner. The h_{fe} minimum of the transistor chosen is taken as 30. When T_1 is off T_2 will be on. Since the saturation voltages are small the base and collector saturation voltages are assumed to be zero. For a silicon device I_{CBO} being small, its impact is neglected. The base voltage V_{B_1} of T_1 is $-V_{BB} \times \frac{R_{BL}}{(R_{B_2}+R_2)}$. The back bias required for cut-off is very small, say, 0.1 V for germanium and 0 V for silicon transistors. Therefore V_{B_1} required is of this order only. However for stable conditions, this can be taken as -1 volt. $-V_{BB}$ is taken as -15 V. Taking the value of R_2 as 100 kilo ohms, R_{B_2} is taken as 6.8 k. ohms. The current I_1 is $\frac{V_{CC}}{R_{C_2}}$ (neglecting the effect of I_{CBO} and assuming the collector saturation voltage as zero). For the transistors chosen the collector current is limited to 7 milli ampere. Therefore the collector resistances are chosen as 2 k. ohms. This leads to $I_1 = 7.5$ ma, $I_2 = 0.13$ ma. Therefore the collector current of transistor T_2, $I_1 - I_2 \doteq 7.37$ ma. Since the current I_2 is small compared to I_{B_1} minimum required, the transistor T_1 will be in cut-off. Similar calculations can be conducted for the other transistor also. The capacitors C_1 and C_2 which are of the order of 100 pfd. are added to speed up the binary action.

Experimental Set Up

Equipments needed

1. Power supply 30V/1A—2 Nos.

2. Function generator—1 No.
3. CRO—1 No.

Components required

1. Transistor CIL 531 or equivalent—2 Nos.
2. Resistance 100 k. ohms 10% $\frac{1}{4}$ W—2 Nos.
3. Resistance 6.8 k. ohms 10% $\frac{1}{4}$ W—2 Nos.
4. Resistance 2 k. ohms 10% $\frac{1}{4}$ W—2 Nos.
5. Resistance 1 k. ohm 10% $\frac{1}{4}$ W—1 No.
6. Capacitor Styroflex 100 pfd—2 Nos.
7. Capacitor ceramic 0.1 mfd—1 No.

Procedure

Connect the circuit as shown in Fig. 30.3. Trigger the on transistor using negative pulse and note the change of the state in the scope. Connect the function generator to the transistor and feed the signal to find the changed state again. Note the wave shape of the binary.

Review Questions

1. Why the speed up capacitors are used in the bistable multivibrator ?
2. Calculate the quiescent value of the circuit voltages and compare it with the experimental value.
3. Discuss the technique of triggering a bistable multimeter.

31

SCHMITT TRIGGER

Theory

The bistable multivibrator or flip-flop is an example of a circuit having two states, which are stable. This circuit is widely used in electronics. Schmitt trigger is a modification of the bistable circuit used for squaring of the waveform. Signal of any shape can trigger a Schmitt Circuit. The output will be a fine square waveform. The biasing for a Schmitt trigger is given through the emitter resistance. When the circuit as shown in Fig. 31.1 is switched on, T_1 will be conducting. The current flowing through the emitter resistor provides necessary biasing conditions. When a sinusoidal waveform is applied to the base of this transistor, transistor T_1 remains in the state of conduction during

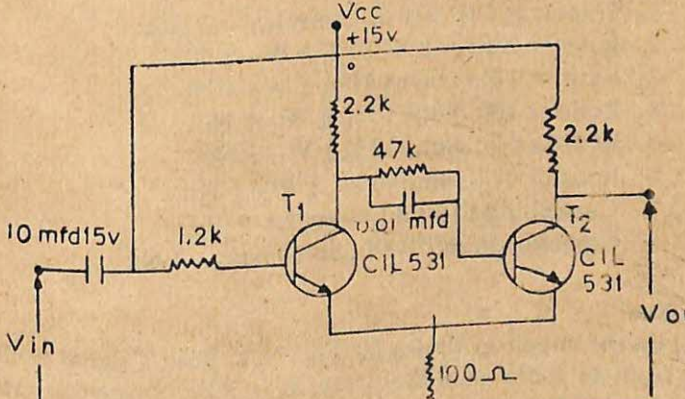


Fig. 31.1

the positive half cycle. During the negative half cycle, the transistor goes in to cut-off causing a transition at its collector. This transition is passed on to the base of T_2 through the coupling capacitor. Transistor T_2 which was in cut-off till now, goes into conduction. Depending upon the input frequency, the number of transitions taking place in the transistors also vary. Number of transitions is equal to the frequency of the input. Since the transistor T_2 goes either from zero to one or one to zero, the output waveform is square wave only. Depending upon the value of emitter resistor and the collector emitter saturation voltage, the dc level varies.

Objective

To study the circuit of Schmitt trigger as a limiting and a squaring circuit.

Experimental Set Up

Equipments needed

1. Power supply 30V/1A--1 No.
2. CRO—1 No.
3. Audio oscillator—1 No.

Components required

1. Transistor CIL 531 or equivalent—2 Nos.
2. Resistor 2.2 k. ohms 10% ¼ W—2 Nos.
3. Resistor 1.2 k. ohms 10% ¼ W—1 No.
4. Resistor 100 ohms 10% ¼ W—1 No.
5. Resistor 5 k. ohms 10% ¼ W—1 No.
6. Resistor 47 k. ohms 10% ¼ W—1 No.
7. Capacitor 0.01 mfd (polyster)—1 No.
8. Capacitor 10 mfd/15V (electrolytic)--1 No.

Procedure

Rig up the circuit as shown in Fig. 31.1. Feed a signal to the input from an audio oscillator, say, at 1 KHz frequency. The voltage should be sufficient enough to trigger the Schmitt circuit, say, 6 volts peak to peak. Observe the waveforms at the output. Vary the frequency of the oscillator and repeat the experiment. In each case observe the waveform and the frequency of the output.

Review Questions

1. What is the quiescent state of the circuit ? Calculate the same from the circuit parameters and compare it with the observed values ?
2. What is the importance of the resistance paralleled to the coupling capacitor from the collector of T_1 to the base of T_2 ?

32

COLLECTOR COUPLED MONOSTABLE MULTIVIBRATOR

Theory

The principle of operation of the collector coupled monostable is same as that for monostable multivibrator which is emitter couple. The output is taken generally from the off transistor. If the collector resistances are unbalanced, the collector voltage waveform will not compliment each other. T_1 is biased so that it is normaly on. Trigger pulses are applied to the base of T_1. The bias voltage $-V_{BB}$ is provided to ensure cut-off on transistor T_2. Without the bias the circuit can be easily triggered and external noise resulting in erratic pulses. When the supply is switched on, the base current flowing to transistor T_1 is adequate enough to keep it saturated. The drop across R_{C_1} resulting from $I_C R_{C_1}$, will drive the collector voltage to nearly zero volt with respect to ground. The voltage divider action of R_{b_2} and R_1 will bias the base of T_2. With this bias T_2 will remain in cut-off state. Since there is no drop across the collector resistance of T_2, the collector of T_2 will be at the supply voltage level itself. This stable state exists during the time interval t_0 to t_1 as shown in Fig. 32.2.

At the instant t_1, a negative spike is applied to the input terminal and the base of T_1 is driven negative. The junction point of R_{b_1} and C_2 is also driven negative. Capacitor T_2 changes to this new voltage. The reverse bias of T_1 makes the impedance of T_1 very high and hence capacitor C_2 can charge through transistor T_2 supply voltage V_{CC} and R_{b_1}. This biases T_2 in the forward direction. Transistor T_2 is switched on and its

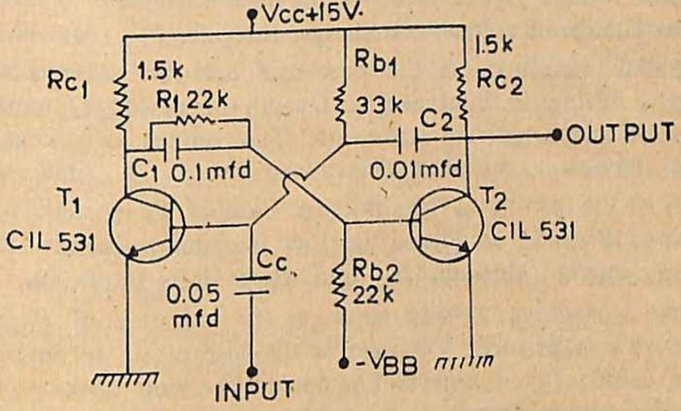


Fig. 32.1

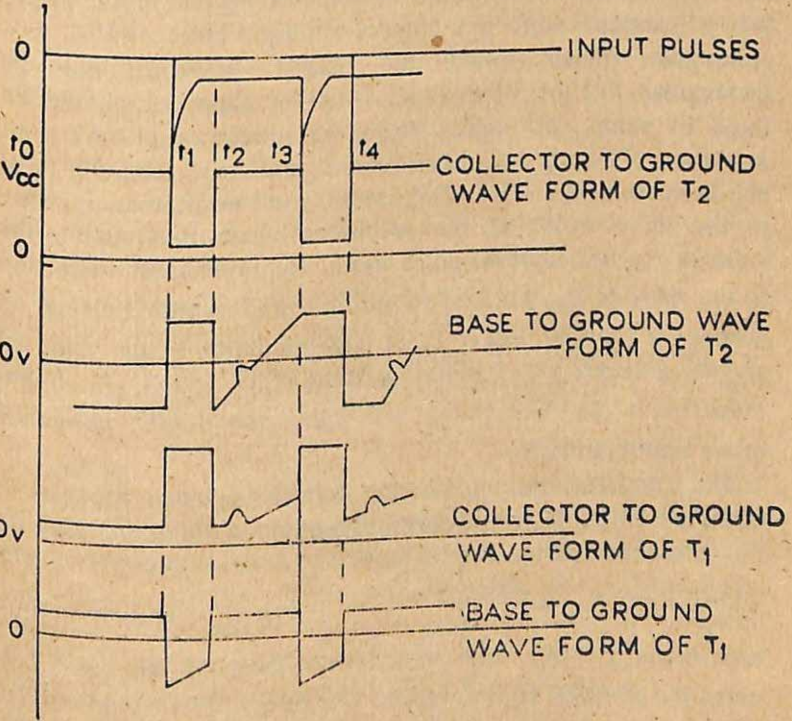


Fig. 32.2

collector voltage goes to zero. At this instant capacitor C_2 sees a sudden change of voltage and charge through R_{b_1}, causing an integrated waveform at the base of T_1 and this becomes more negative during the interval t_1-t_2. During this period T_1 remains at cut-off and T_2 goes to saturation. The output is a negative pulse having a duration determined by $R_{b_1}C_2$ time constant. At the instant t_2, the voltage at base of T_1 permits conduction. When T_1 conducts, its low impedance permits more biasing current through R_{b_1} and drives it to saturation. This causes a negative voltage surge at the collector of T_1. This negative voltage surge is coupled to the base of T_2 through C_1. This causes T_2 to cut-off. The current carrying capacity of C_1 sees the voltage changes at the collector of T_1. The output of the circuit is assymetrical rectangular waveform for a sine wave input of reasonable amplitude. To some extent the input amplitude adjustment results in a control of output pulse widths. For rectangular trigger inputs, the output waveform will be rectangular. For low PRFs input coupling capacitor should be large in value. At higher PRFs the squareness of the output waveform depends on transistor rise time, delay time, fall time, etc. Increase in the value of R_{b_1} and C_2 will result in an increase in the pulse width of the output waveform. Reduction in the value of R_{b_2} will increase pulse width. An appreciable reduction in the value of R_{b_2} will lead to multiple and erratic pulsing on account of reduced bias to T_2. A large reduction in the value of R_{c_2} will generate a step voltage pattern at the output. A similar reduction in the value of R_{e_1} will widen the output pulse and cause erratic pulsing.

The transistors chosen for the collector-coupled monostable multi are CIL 531 or equivalent. Assuming a minimum beta of 30, saturation current can be limited to a reasonable value 10 ma. This means $R_{c_1} = \frac{(V_{CC}-V_{sat})}{I_{sat}} = \frac{(15-0.3)\,V}{10\text{ ma}} = 1.47$ k. ohms approximately. We can take the value of R_{c_1} as 1.5 k. ohms for practical consideration. The base current required for this transistor is 0.33 ma. This is supplied through the resistor R_{b_1}. Base current is equal to $\frac{(V_{CC}-V_{BEsat})}{R_{b_1}}$. From the value of the base current calculated earlier R_{b_1} can be determined as nearly 47 k. ohms. In order to keep the transistor always in conduction the value of R_{b_1} is chosen as 33 k. ohms. When T_1 is on, the voltage at the collector of T_1 is almost zero. To keep T_2 off R_{b_2} has to be returned to a negative voltage. This voltage is chosen to be around 3 volts. To provide for suitable discharge time constant R_{b_2} is chosen as 22 k. ohms, the value of R_1 is chosen as 22 k. ohms. The resistor R_{c_2} is chosen as equal to R_{c_1}. The charging capacitor C_1 is chosen as 0.1 mfd. The capacitor C_2 is chosen as around 0.01 mfd. The coupling capacitor is chosen as 0.05 mfd.

Objective

To study the characteristic of collector coupled monostable multivibrator.

Experimental Set Up

Equipments needed

1. Power supply 30V/1A—1 No.
2. CRO—1 No.
3. Function generator—1 No.
4. Power supply 15V/100 ma—1 No.

Components required

1. Transistor CIL 531 or equivalent—2 Nos.
2. Resistor 33 k. ohms 10% ¼ W—1 No.
3. Resistors 22, 15 k. ohms 10% ¼ W—2 Nos. each.
4. Capacitors 0.1, 0.05, 0.01 mfd (polyster)—1 No. each.

Procedure

Connect the circuit with the values shown in Fig. 32.1. Connect the CRO to the output transistor and feed a signal at the input. Observe the output waveform. Vary the input frequency and note the variations in the output. Repeat the experiment for input of sine and square waves at different frequencies. Observe the waveform at the collector of the other transistor and also observe the waveforms at the bases of the transistors.

Review Questions

1. Which transistor is normally in a state of conduction ?

Theoretecally calculate the collector current and base current.

2. Describe in detail how the transition from stable state to quasi-stable takes place.
3. Calculate the period of time that the monostable multivibrator will remain in its quasi-stable state using the approximate formula $T = 0.69\ RC$.

33

EMITTER COUPLED MONOSTABLE MULTIVIBRATOR

Theory

Unlike the binary circuit, the monostable has got only one permanent stable state and quasi-stable state. In the monostable, a triggering signal is required to effect a transition from stable state to that of quasi-stable. The circuit will remain in the quasi-stable state for a period which is longer than the time taken for transition between the states. The circuit will come back to the stable state from its quasi-stable state without any triggering signal. The emitter coupled monostable multivibrator is biased to clamp one transistor in the saturation region. The normally on transistor will remain in this state indefinitely till the off transistor is triggered to the on state. After some pre-determined interval, the circuit will return to its normal state until it is again triggered.

The common resistor R_E provides the necessary feedback for the circuit to operate. This avoids the need for another negative supply. The transistor T_2 will be forward biased so that it remains in saturation. The voltage drop across R_E is sufficient enough to reverse bias T_1 and keep it in the cut-off region. R_{c_2} is chosen such that it permits higher saturation current in T_2. R_{c_1} is chosen so that the saturation current is kept smallar as compared to the saturation current of T_2. The circuit will remain in this state until T_1 is triggered through an external signal as shown in the Fig. 33.1. The negative going pulses fed to the base T_1 to maintain the base-emitter junction in the reverse biased state. The positive going pulses will tend to forward bias T_1. The transistor T_1 cannot conduct until the base is positive

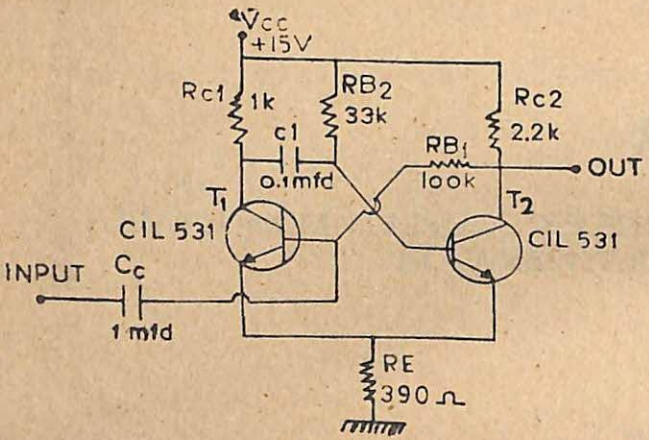


Fig. 33.1

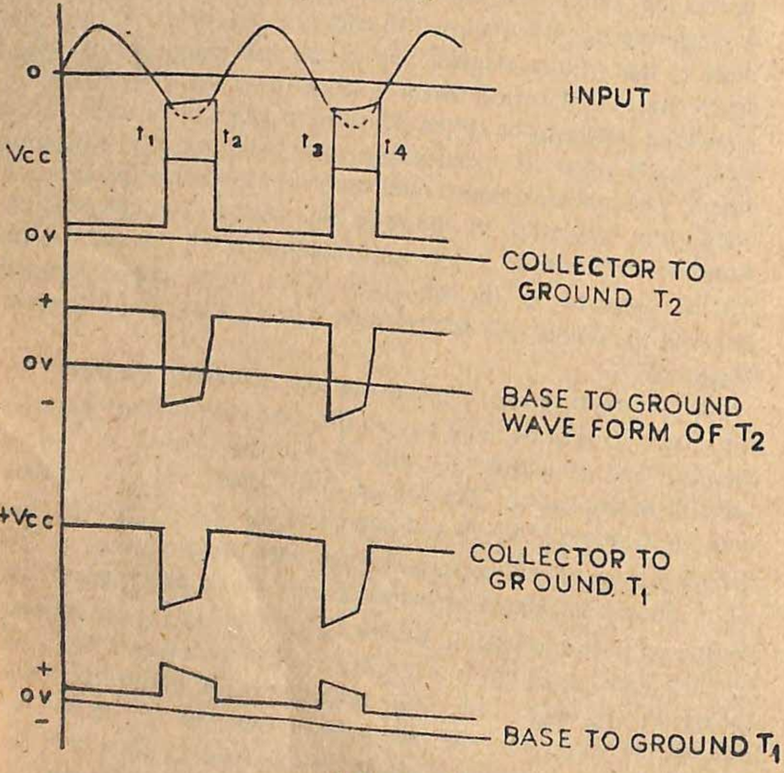


Fig. 33.2

enough with respect to the voltage drop across R_E. This is to say that the amplitude of the signal should be sufficiently large to bias the transistor T_1 towards conduction. This occurs at the point T_1 as shown in Fig. 32.2. As soon as T_1 conducts, the input generator sees a low impedance which produces a loading effect on the input generator. At the same time collector current through R_{C_1} increases, producing a negative going voltage seep at the collector of T_1. This step is coupled with the base of T_2 tending to reverse bias T_2. This reduces the current through T_2. This causes lower drop across R_E. This reduced voltage across R_E reduces the reverse bias voltage of T_1. The feedback causes results in an almost instantaneous switching on of T_1 and switching off T_2.

Immediately after the instant T_1 as shown in Fig. 33.2, capacitor C_1 starts discharging through the loops T_1, R_E, R_{B_2}. Though the main discharging is through T_1, there is a small increase in the drop across R_{C1}. At some point, the current through T_1 begins to decrease. This generates a forward biasing on the base of T_2. At the instant T_2 shown in Fig. 33.2, the base voltage of T_2. reaches a value enabling T_2 to conduct. Through R_E, T_1 is reverse biased again and transistor T_1 goes into cut-off and the original state of T_0 is restored at the instant T_2. The output signal voltage is almost proportional to $\frac{R_{C_2}}{R_{C_2}+R_E}$. Since V_{CC} determines the saturation current, the output voltage is proportional to supply voltage. The coupling capacitor C_c has a say on the shape of the input waveform. Large capacitances are desirable for low pulse repetition frequency (PRF). The value of R_{B_1} will affect the bias on T_1 and the amplitude of input pulses appearing in the base of T_1. Smaller values of R_{B_1} will require larger input voltages for equal output amplitudes. The resistor R_{B_2} along with capacitor C_1 will determine the recovery time (time constant) of the circuit. That is the smaller the value of R_{B_2}, the smaller is the time constant. Reducing the discharge time of C_1 results in a reduced width of the output pulses. Various waveforms can be used to trigger the monostable. The output will always be rectangular except for excessively large input.

The charging circuit consists of C_1, R_{B_2} and R_{C_1}. Their values are chosen as 0.1 mfd, 33 k. ohms and 2.1 k. ohms respectively. The values of R_{B_1}, R_{C_2}, R_E and C_C are chosen as 100 k. ohms, 2.1 k. ohms, 390 ohms and 1.0 mfd respectively. When transistor T_2 is on, it tends towards saturation. For a V_{CC} of +15 V, the current I_C will be around 10 ma. The drop across R_E tends towards 3.9 V. R_{B_2} provides the necessary bias current for T_2. For a h_{fe} of 30, the base current for saturating the transistor T_2 is 0.33 ma. R_{B_2} is able to provide this much current. So T_2 will always go to the saturation. Now at the collector of T_2, the voltage available is the drop across $R_E+V_{CE_{sat}}$. Neglecting the $V_{CE_{sat}}$ the voltage at the collector of T_1 is $I_E.R_E$ which is around 3.9 V in this case. That means the transistor T_1 has its emitter and base almost in the same potential. The higher value of R_{B_1} (100 k. ohms) is sufficient enough guarantee to see that T_1 is kept in the off condition. The amplitude of the pulse required to trigger T_1 into on condition is well above 3.9 volts. As T_1 is triggered into conduction C_1 gets charged through R_{B_2} and T_1. C_c is chosen as 1.0 mfd to enable distortion-free signal for triggering the monostable multivibrator.

Objective

To study the characteristic of emitter coupled monostable multivibrator.

Experimental Set Up

Equipments needed

1. Power supply 30V/1A—1 No.
2. CRO—1 No.
3. Function generator—1 No.

Components required

1. Transistor CIL 531 or equivalent—2 Nos.
2. Resistors 390 ohms, 1, 2.1, 33, 100 k. ohms, 10% ¼ W—1 No. each.
3. Capacitors 1.0, 0.1 mfd (polyster)—1 No. each.

Procedure

Connect the circuit as shown in Fig. 33.1 and feed a signal of suitable amplitude and frequency at the input. Observe the waveform in the CRO at the output point. Note the on and off times by varying the signal frequency. Repeat the experiment by changing the value of C_1 and R_{B_1}.

Review Questions

1. Explain how the biasing voltage is generated in the circuit.
2. Discuss the transition of the states in the monostable multivibrator.

34

ASTABLE MULTIVIBRATOR COLLECTOR-COUPLED

Theory

Multivibrator circuit consists of two overdriven amplifiers connected in such a manner that each provides the input signal to the other. In the normal operation only one amplifier is in the on state and the other in the off state. The switching from off to on takes place on a pre-determined rate depending upon the time constant of the resistance-capacitance coupling. The astable multivibrator is a free running oscillator which generates rectangular waveforms. The astable multivibrator is frequently forward biased with zero fixed bias which enables it to have an operating point at cut-off in the absence of a signal. The load resistances R_{c_1} and R_{c_2} are selected such that the transistor is in the saturation point giving the maximum desired collector current. The bias resistors R_{b_1} and R_{b_2} are chosen to provide the sufficient base currents to ensure collector saturation. The coupling capacitors C_1 and C_2 determine the time constants along with R_{b_1} and R_{b_2} and control the switching action.

The initial application of the supply voltage will cause a charge flow through both the transistors. Since it is impossible to build circuits with the transistor T_1 circuitry is identical to that of transistor T_2 circuitry, the collector voltage at one of the transistors will be more positive with respect to the other. Assume that the current at T_1 is greater, resistors R_{b_1} and R_{b_2} are required to provide only microamperes of base current. The base voltages being small and negative and tend to bias base-emitter junctions in the forward direction. Both capacitors starting from zero charge, will try to charge to the voltage between collector and base terminals, C_1 with charge lower than C_2. Charging C_2 to the more positive potential at the collector of T_2 produces a greater bias on base of T_1 and hence increases the collector current through T_1. This drives T_1 further and makes it saturated and driving T_2 more negative and finally to cut-off. At the end of the time constant of the RC the operation reverses driving T_1 more negative and T_2 on condition. The collector and back waveforms of the transistors are shown in Fig. 34.1.

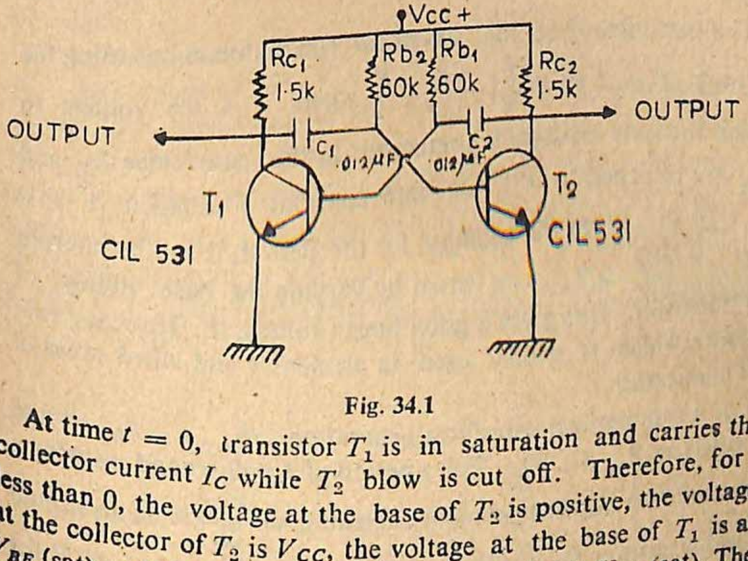


Fig. 34.1

At time $t = 0$, transistor T_1 is in saturation and carries the collector current I_C while T_2 blow is cut off. Therefore, for t less than 0, the voltage at the base of T_2 is positive, the voltage at the collector of T_2 is V_{CC}, the voltage at the base of T_1 is at V_{BE} (sat) and the voltage at the collector of T_1 is V_{CE} (sat). The capacitor C_2 charges through R_{b_1} and the voltage at the base of

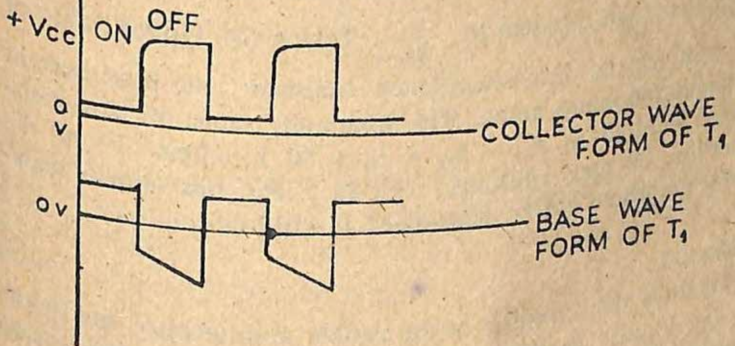


Fig. 34.2

T_2 rises exponentially towards V_{CC}. At $t = 0$, the base of T_1 becomes sufficiently positive and T_2 conducts. As T_2 goes to saturation the collector voltage of T_2 rises to V_{CE} (sat). The rise in the collector voltage of T_2 causes an equal fall in the base voltage of T_2 through the capacitor coupling network. This fall in the base voltage of T_1, cuts off T_1 and its collector voltage rises towards V_{CC}. This rise in the collector voltage of T_1 is coupled through capacitor C_2 to the base of T_2. This causes and overshoot in the base voltage of T_1 as shown in the waveform (Fig. 34.2).

The periodicity of the waveform can be found out using the formula $T = 2\,RCln\left(1 + \frac{V_{CC}}{V}\right)$ where V is the voltage to which the base resistors are returned. In this case since R_{b_1} and R_{b_2} are returned to V_{cc}, the time constant $T = 2RC\ln(1 + 1)$ $= 1.38\ RC$. From the equation for the period, it can be inferred that the frequency can be varied by varying the base voltage of the transistor. This gives a good linear voltage to frequency conversion which is widely used in elementry and allied areas of communication.

For a symmetrical waveform generation; R_{c_1}, C_1, R_{b_1} should be equal to R_{c_2}, C_2, R_{b_2}. For a period of 1 millisecond waveform the maximum allowed collector current $I_c = \frac{V_{CC}}{R_c}$. The maximum collector current can be limited to 10 ma and V_{CC} to + 15 V for CIL 531 or equivalant transistor. This leads us to the value of R_c as 1.5 k. ohms. To ensure saturation the base current I_b should be greater than or equal to $\frac{I_c}{h_{fe}}$. Taking the typical value of h_{fe} as 40 for the above-mentioned transistor, the base current becomes 250 micro amps. The minimum value of base resistance required is $R_b, = h_{fe} \times R_c = 60$ k. ohms. From the equation of time constant $T = 1.38 \times R_bC$, the value of capacitance required can be determined as 0.012 mfd.

Objective

To study the waveform of the astable multivibrator and modify the circuit to know the voltage to frequency conversion aspect of the circuit, calculation of linearity.

Experimental Set Up

Equipments needed

1. Oscilloscope—1 No.
2. Power supply 30V/1A—2 Nos.
3. Frequency counter—1 No.

Components required

1. Transistor CIL 531 or equivalent—2 Nos.
2. Resistors 60, 1.5 k. ohms 10% ¼ W—2 Nos. each.
3. Capacitors 0.012 mfd (polyster)—2 Nos.

Procedure

Make the connections as shown in Fig. 34.1 and switch on the power supply keeping V_{CC} at + 15 Volts. Observe the collector and base waveforms in the CRO. Note the period of the waveforms. Draw the waveform on a graph sheet. Compare the period of the waveform theoretically calculated with that of the practical value observed. Vary the value of R_b and C and observe the waveform and note the period. Modify the circuit as shown in Fig. 34.3. Vary the voltage V_{bb} in steps of 1 V starting from 0 V and observe the output frequency counter. Care should be taken to see that V_{bb} never exceeds the value of V_{CC}. Draw a curve connecting the output frequency and input voltage V_{bb}, determined linearly from the graph.

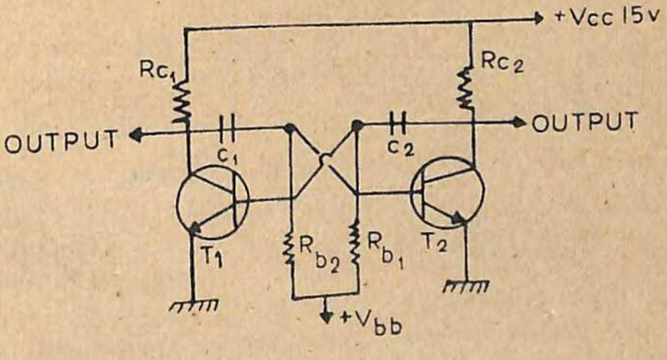


Fig. 34.3

Review Questions

1. Compute the period of repetitive waveform produced for

a particular value of coupling capacitor and compare the same with the observed value.

2. Whal should be the ideal waveforms of the collector and the base of the astable circuits ?
3. Discuss the voltage to frequency conversion action of the astable multivibrator.

35

PULSE TRANSFORMER

Theory

Pulse transformers find wide application in the waveshaping, triggering and scores of other activities involving pulses. A pulse transformer is used for differentiation of pulses, used as a coupling element between pulse amplifiers used for inversion of the pulse polarity, to change the amplitude and impedance level of a pulse, and to provide dc isolation between a pulse source and a load.

The representation of a transformer turns ratio through equation is done as a ratio of turns, voltage, current or inductance as shown below. Turns ratio $= \frac{N_s}{N_p} = \frac{V_s}{V_p} = \frac{i_p}{i_s} = \sqrt{\frac{L_s}{L_p}}$ where N_s stands for secondary turns, N_p for primary turns, V_s for secondary voltage, V_p for primary voltage, i_p for primary current, i_s for secondary current, L_p for primary inductance and L_s for secondary inductance.

Figure 35.1 shows the symbolic representation of a transformer. The letter M designates the mutual inductance which is related to the coupling between the primary and secondary windings. The degree of coupling is determined by the core material and shape of the transformer as well as the manner in which the two windings are placed with respect to each other. Coefficient of coupling is expressed as $k = \frac{M}{\sqrt{L_p.L_s}}$. Practical transformers have magnetic leakage, resistance in windings, and distributed capacitance. In pulse transformer these are very important factors in determining the shape of the pulse. When a

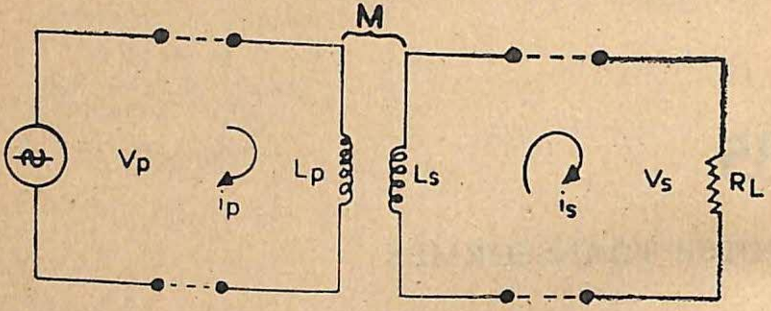


Fig. 35.1

step input is given to the primary of a pulse transformer the equivalent RLC circuit will be excited into an oscillation. The frequency of oscillation will be quite constant regardless of the input pulse rate. If pulses are applied at the oscillation frequency, the secondary output voltage peaks will exceed the input voltage peaks. At resonant pulsing, the turns ratio of the transformer has no meaning, but the *Q* of the circuit assumes great importance. As the *Q* of the transformer equivalent circuit increases, the amplitude of the oscillation also increases.

Just as resistance any resonant circuit affects its *Q*, transformer resistance affects the *Q* of the circuit also. The leakage inductance reduces the magnitude of the pulse and the capacitances associated with the transformer affect the resonant frequency.

If the resistance in a resonant circuit is neglected, the resonants frequency of the circuit is given by $f = \frac{1}{2\pi\sqrt{LC}}$. For the pulse transformer *L* is not the inductance that can be measured by an impedance bridge. Likewise *C* is not purely the capacitance between the primary and secondary windings. The equivalent *L* for the oscillation in the pulse transformer is a function of magnetic loops. The calculation of this is a quite involved process and the value depends on the degree of magnetic saturation of the core. The measurement and study of the value of *L* and *C* plays an important role because they determine the rise time and decay time of pulses at the output terminals.

The resonant frequency of the transformer secondary can be determined by applying a constant voltage at the input at different frequencies and observing the sharp increase in the secondary output corresponding to the resonant condition. This resonant frequency f_o is determined by the effective secondary inductance L_s and distributed capacitance C_D. If a known capacitance C_1 is connected across the secondary winding, a lower resonant frequency can be noticed at f_1. At still larger value of capacitance C_2 the frequency of resonant gets shifted to lower value f_2. From the changes in frequency associated with the capacitance changes, it is possible to compute the effective secondary inductor L_s with reasonable accuracy using the formula

$$L = \frac{f_1^2 - f_2^2}{(2\pi f_1 f_2)^2 (C_2 - C_1)}$$

The formula assumes L as constant. The distributed capacitance C_D can be determined using the formula $f_o = \frac{1}{2\pi \sqrt{L_s C_D}}$. The value of L_s will be considerably less than the secondary inductance measured using the impedance bridge. In this manner the effecttive primary inductance L_p can also be determined. However, these secondary and primary inductances bear the same ratio as between the values measured using the impedance bridge for secondary and primary side. These values of inductances, determine the shape and frequency of the pulse waveform apart from the factors like the magnetic core material, the type of winding, turns ratio, etc.

Objective

To study the parameters and behaviours of pulse transformer.

Experimental Set Up

Equipments needed

1. CRO—1 No.
2. Pulse Generator—1 No.

Components required

1. Assorted values of capacitors
2. Ferrite toroidal magnetic core—1 No.
3. Copper wire of SWG 42—some quantity.

Procedure

Choose a proper type of ferrite core available in the laboratory. Wind, in bifilar fashion, about 20 turns in the primary and 60 turns in the secondary. Connect the function generator to the primary as shown in Fig. 36.1. Look for the output at the secondary for constant input voltage of 5 V_{pp} at various frequencies. Note the value of the frequency at which the resonance occurs. Repeat the experiment by connecting capacitors of different values across the secondary. From these values determine the effective value of L_s and C_D using the formula

$$f_0 = \frac{1}{2\pi\sqrt{L_S C_D}}$$

Note the amplitude and shape of the pulses. Experiment can also be done for higher turns ratios also.

Review Questions

1. What magnetic properties of the core determine the frequency limitation of the pulse transformer ?
2. Discuss the reasons for the pulse amplitude behaviour with respect to frequency.

36

BLOCKING OSCILLATOR

Theory

Blocking oscillators are widely used in radars, TVs, in counting circuits, etc. The blocking oscillator employs a transformer to provide feedback from output to input of an amplifier. In a way it is an inductively coupled oscillator and relaxation oscillator combined together. This circuit generates a variety of waveforms simultaneously in the various parts of the circuit.

The important device in the Blocking Oscillator is a pulse transformer. The leakage inductance, distributed capacitance, resistance, turns ratio, core magnetisation and winding inductance play a vital role in the design of Blocking Oscillator. The time constant, L/R, of the pulse transformer is a very important factor. An abrupt change in the current through the inductance causes an induced voltage in it. A uniformly increasing current through the inductor generates a constant induced voltage across the inductance. The voltage appearing across the winding of the pulse transformer will appear across the other winding multiplied by the turns ratio. Referring to the common emitter configuration of blocking oscillator shown in Fig. 36.1, the primary winding is in the collector-emitter loop, secondary winding is in the base-emitter loop. The voltage and current in the loops at any instant will be determined by the transformer turns ratio and phase inversion. The dots at the ends of the pulse transformer indicate that corresponding points will be simultaneously positive and negative whenever a varying current flows in one of the windings. This connection of the pulse transformer to the transistor ensures a positive feedback filfulling the conditions for

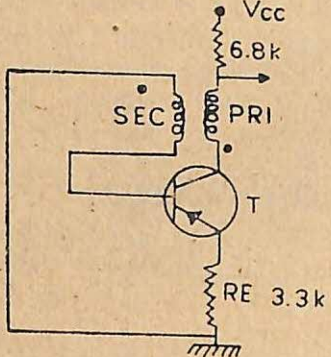


Fig. 36.1

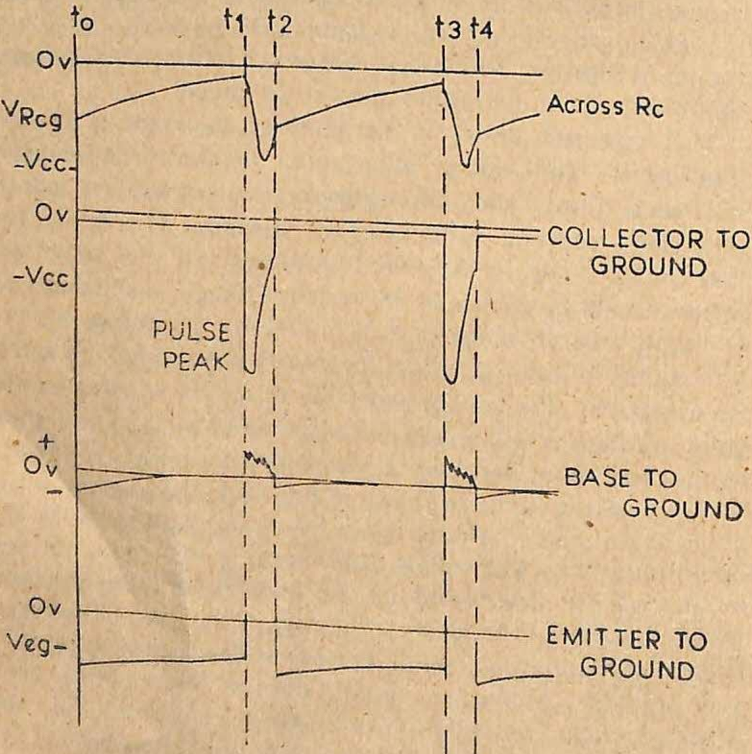


Fig. 36.2

oscillation. As the collector goes positive, the base goes negative. Since the common-emitter amplifier inverse the input signal in the output the connections shown in the Fig. 36.1 will produce positive feedback. To ensure greater stability in operation, the emitter resistance R_E is unbypassed. Resistor R_E provides negative feedback to the base emitter loop. Since the base bias is zero, the circuit behaves as an astable oscillator.

Referring to Fig. 36.2, at the instant of switching on the power to the circuit $t = t_0$, collector current starts to flow and increases at the rate determined by L/R time constant of the pulse transformer primary and the resistor R_C. Since the current increase rate is uniform, counter emf across the primary inductance will remain constant, keeping the collector to ground voltage at zero level. The rising collector current magnetises the pulse transformer and produces a magnetic field which also cuts the secondary winding. The voltage across the primary is relatively constant and hence there will be very little change in the base to ground voltage. The emitter voltage will reach a negative value before the instant t_1 is reached, even though V_{CE} will remain near zero. At the instant t_1 collector current reaches saturation level and the rate of change of current becomes zero causing the collapsing of the magnetic field. The collapsing field generates negative voltage which is much larger than the applied voltage V_{CC} because the rate of change of current is larger. To protect the transistor from such sudden voltages a resistor and a diode in series across the primary are generally used. In this circuit since R_E and R_C provides enough protection, abovesaid combination is not required. The collector to ground voltage at time t_1 reaches a large negative value. The large negative going voltage is stepped down which produces a positive going pulse to the base of the transistor. This causes a cut-off state to the transistor. At this state, the transistor presents a high resistance in the primary of the pulse transformer as long as the primary inductance is returning energy to the circuit. The energy is stored in the transformer magnetic field. The emitter voltage also turns positive. During the intervel t_1 to t_2 the decrease in the bias current and increasing collector current cancel each other keeping the voltage across R_E constant. The decaying mangetic field allows the collector voltage to return to zero. Base voltage also approaches zero volt condition to enable the transistor to conduct.

At the instance t_2, the base swings beyond zero and becomes slightly negative causing the collector current to increase at the rate determined by the time constant of the transformer. The voltage across R_E suddenly becomes negative. During the interval t_2 to t_3, the voltage at R_C increases like a ramp as shown in Fig. 36.2. The increasing collector current causes a gradually positive going voltage across R_E. Similar trend is noted at the base to the ground point also. At t_3, the cycle repeats as at t_1 and oscillator continues pulsing at the rate determined by the circuit parameters.

Objective

To study the various waveforms generated by the blocking oscillator circuit.

Experimental Set Up

Equipments needed

1. CRO – 1 No.
2. Power supply 30V 1A—1 No.

Components required

1. Transistor CIL 231 or equivalent—1 No.
2. Pulse Transformer Secondary to primary turns ratio 1:5—1 No.
3. Resistors 6.5, 3.3 k. ohms 10% ½ W—1 No. each

Procedure

Rig up the curcuit as shown in Fig. 36.1. Keep the power supply voltage around −15 V and switch on the supply. Connect an oscilloscope probe to the various points like the collector, emitter, base and the resistor R_C with respect to ground and study the waveform at all these points. Repeat the experiment by connecting $R_C = 10$ k. ohms and $R_E = 4.7$ k. ohms.

Review Questions

1. What factors determine the sharpness of various waveforms in the blocking oscillator ?
2. Discuss the switching speed requirements of the transistor used in the blocking oscillator.
3. How the waveforms look like when the NPN transistor and positive supply voltage are used?

37

SYNCHRONISATION TECHNIQUE IN ASTABLE MULTIVIBRATOR

Theory

When a timing pulse is applied externally to one transistor or simultaneously to both transistors of an astable multivibrator, it causes the multivibrator to switch stable states at the same frequency with which this and subsequent timing pulses are applied. These pulses applied to the base of one or both the transistors of the astable multivibrator are known as the synchronising pulses. When positive pulses are applied to the base of T_2, these triggers may produce synchronisation by establishing the exact instant at which T_1 comes out of cut-off. If negative pulses are applied to the base of T_1, then, when T_1 conducts, these pulses will be amplified, inverted and then appear as positive pulses at the base of T_2. Hence, again the pulses will establish the instant when T_2 comes out of cut-off. A capacitor is used to inject the synchronisation signal into the base of the transistor. The value of the capacitor is not very critical. To differentiate a given square wave into pulses and then to select positive going pulses, capacitor and diode are used.

Experimental Set Up

Equipments needed

1. Power supply 30V/1A—1 No.
2. CRO—1 No.
3. Function generator—1 No.

Components required

1. Transistor CIL 531 or equivalent—2 Nos.
2. Capacitors 0.03 mfd (Polyster)—2 Nos.
3. Capacitors 0.33 mfd, 0.1 mfd (Polyster)—1 No. each
4. Diode CD 31 or equivalent—1 No.
5. Resistors 1.2, 15 k. ohms 10% $\frac{1}{4}$W—2 No. each

Procedure

Rig up the circuit as shown in Fig. 37.1. Keep the supply voltage at +15 V and switch on the circuit. Connect the CRO probe to the collector of T_2 and see the waveform in CRO. See the base waveform also. Note the frequency of the oscillation. Now connect the function generator to the cirucit and keep the function switch to square wave and the frequency near the frequency of oscillation of the astable. See the waveform of the astable multi at the collector of T_2. Adjust the amplitude of the function generator to obtain stable synchronisation. See the waveform at the base also.

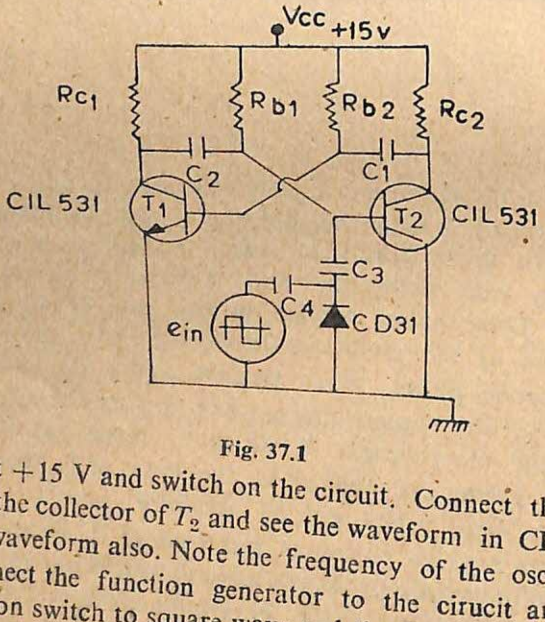


Fig. 37.1

Review Questions

1. What is the effect of using negative pulses in synchronisation ?
2. Discuss synchronisation of astable multivibrator using sinewave.
3. What is the relationship between the amplitude and frequency of the synchronisation of pulse ?

38

CHARACTERISTICS OF A SERIES REGULATOR

Theory

Series regulator circuits are widely used in the design of power supplies, used in laboratories and in various instruments. The series regulator has to give a constant output even if the input voltage fluctuates widely. A transistor is used as the series element which handles the output power. The block diagram of a simple series regulator is as shown in Fig. 38.1. This consists of four blocks as shown. The series element controls the output. The output is sensed by the comparison element and compares with the reference voltage shown in the block and the error that follows is amplified by the error amplifier which in turn corrects the series element to give constant output. Even if the input

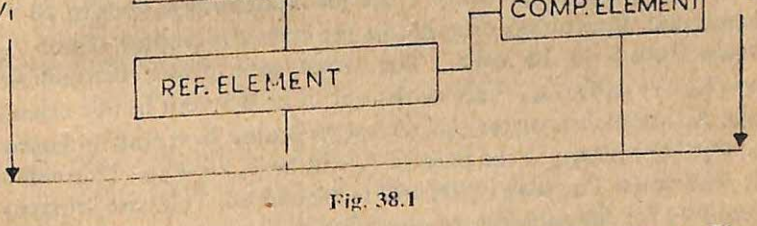


Fig. 38.1

voltage varies, the output is maintained at a constant value by this circuit.

A series regulator can be designed in the following manner. The conditions are (*i*) input voltage varies from 15 to 20 volts, and (*ii*) the output requirement is 10 volts. The basic circuit is shown in Fig. 38.2. Let the output current required to be around 50 milliamperes. The transistor T_1 acts as the series regulator, T_2 acts as the error detecting amplifier, z_1 acts as the reference voltage, R_3 and R_4 acts as the comparison circuit. R_1 and R_2 are used in the amplifier and reference circuit to provide necessary gain and limit the current respectively. Since the input voltage goes to 20 V maximum, the voltage drop across the collector emitter region T_1 varies from 5 to 10 volts. The worst case power dissipation $= (V_{in} - V_{out}) \times I_{max}$. This works out to be 0.5 watt in this example. A suitable transistor, 2N 697, with proper heat sink is chosen at T_1. The voltage at the base of T_1 will be $V_{out} + V_{BE}$. This value is 10.6 volts. The beta of 2N 697 is around 60. The base current required for the satisfactory operation of T_1 is given as the ratio of output current to the beta of the transistor. In this example this works out to be 0.8 ma. The minimum drop across the resistor R_1 will be 4.4 volts. Allowing a current of 1.2 ma to flow through R_1 will suffice to provide the bias current for T_1. Therefore, R_1 is taken as 3.6 k. ohms, which is the ratio of the minimum drop across R_1 to 1.2 ma current. Selection of T_2 is on

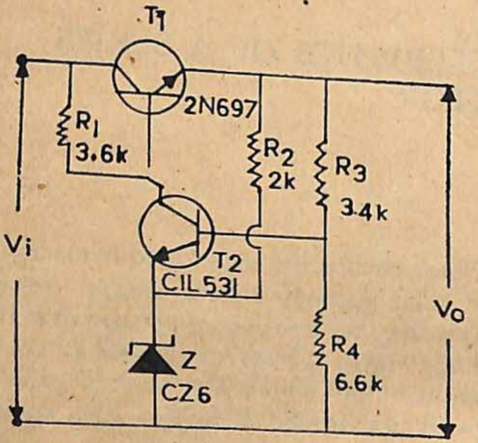


Fig. 38.2

the basis of the amplification capabilities and the current delivery capability. Transistor CIL 531 whose beta is 60 on an average is chosen as the element for T_2. For the reference a zener of 6 volts break voltage is chosen to provide a constant voltage reference which is free of any temperature variation. The zener requires a minimum of 2 ma current to maintain its voltage. The resistor R_2 provides the necessary current path for this. The value of R_2 therefore works out to be 2 k. ohms. The voltage of the base of T_2 has to be 6.6 volts in order to keep the transistor in the conduction state. The base current required for T_2 is determined from the knowledge of its collector current and beta. From this it can be determined that the base current required is 20 micro amperes. A current flow of 1 milliampere through R_3 and R_4 will prove this base current to T_2 without appreciably loading the sampling circuit. From this the sum of R_3 and R_4 can be determined as 10 k. ohms. Since the base voltage has to be maintained at 6.6 volts the following calculations can be carried out and the values are arrived at as $R_4 = 6.6$ k. ohms and $R_3 = 3.4$ k. ohms.

Objective

To study the voltage regulator characteristics.

Experimental Set Up

Equipments needed

1. Power supply or variable power source—1 No.
2. Multimeter—1 No.
3. Rheostat 0 to 1 k. ohm—1 No.

Components required

1. Transistors 2N 697, CIL 531 or their equivalent —1 No. each
2. Resistors 3.6, 2, 6.6, 3.4 k. ohm 10% $\frac{1}{4}$ W—1 No. each
3. Zener Diode CZ 6 or equivalent—1 No.

Procedure

Wire up the circuit as shown in Fig. 38.2. Give the input voltage at 15 volts and note the output voltage. Load the circuit to draw a current of 50 ma. Note the output voltage under loaded condition. Find out the difference in the output between the loaded condition and no-load condition. Calculate the load regulation using the formula,

$$\text{load regulation} = \frac{V_{0(\text{no load})} - V_{0(\text{full load})}}{V_{0(\text{no load})}} \times 100\%$$

Vary the input to 20 volts and observe the regulations as above. Connect the probe of an oscilloscope to the output of the power supply and find the ripple output when in full load condition. Compare this with the ripple output of the unregulated supply at the input. Record the readings.

Review Questions

1. Explain the output impedance of a power supply. How is it calculated ?
2. Determine the ripple reduction factor of the power supply circuit.
3. What is meant by line regulation ?

39

SILICON CONTROLLED RECTIFIERS

Theory

Semi-conductor devices which are used primarily as on-off switches find very wide applications in industry. SCR and triac are very popular unidirectional and bilateral thyristors. A simplified diagram of SCR is shown in Fig. 39.1. The arrowhead shown in Fig. 39.1 (b) determines the conventional current flow in one direction only, that is between the switch terminals anode and cathode. When SCR is turned on, by the application of suitable signal between gate and cathode, it behaves as a closed switch. Once the gate turns on the SCR, it ceases its control over it. To turn the SCR off, the load current must be forced to zero. Fig. 39.2 illustrates this action. In short, the SCR conducts only when the anode is positive with respect to cathode and at the same time gate gets sufficient positive voltage with respect to cathode for triggering action. Only when the anode current is interrupted and the gate drive removed the SCR will be *off*.

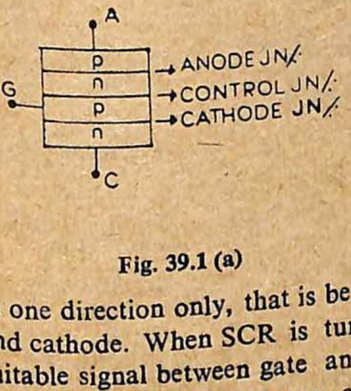


Fig. 39.1 (a)

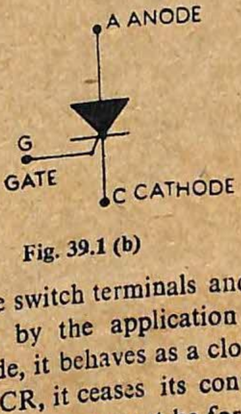


Fig. 39.1 (b)

The Fig. 39.3 shows a true transistor analogy for the SCR. Fig. 39.3 (d) gives the flip-flop arrangement of the transistor.

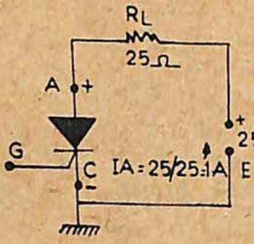


Fig. 39.2 (a)

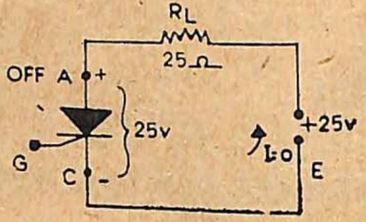


Fig. 39.2 (b)

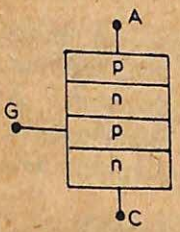


Fig. 39.3 (a)

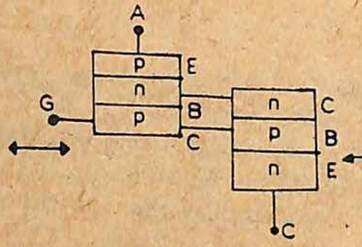


Fig. 39.3 (b)

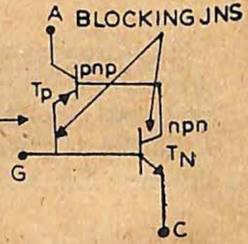


Fig. 39.3 (c)

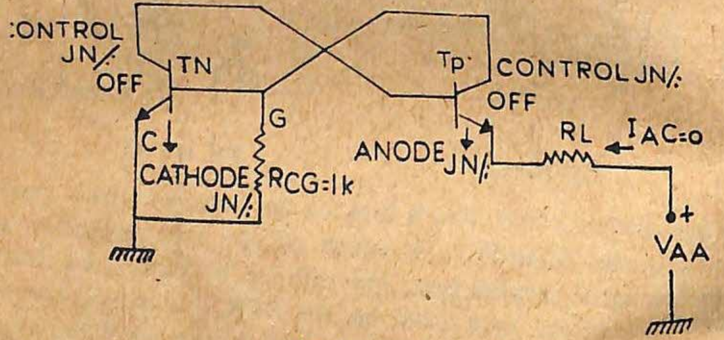


Fig. 39.3 (d)

Here the SCR is *off* or in a forward blocking condition when V_{AA} reverse biases the blocking junction transistor T_N. Resistor R_{GC} is connected to give a low resistance path between gate and cathode for low current. This path bypasses internal leakage currents and external noice signal away from the cathode junction to minimise uncontrolled turn on. If V_{AA} is reverse in polarity both cathode and anode junction gets reverse back and controlled junction forward bias. This condition is called reverse blocking.

To turn the SCR *off* stage to *on* stage the gate should be made positive with respect to cathode. The minimum gate voltage, V_G, is called the gate triggering voltage and this will be of the order of 0.6 volt to forward bias the silicon *pn* junction. When the applied gate voltage is equal to the gate triggering voltage, gate current flows into the base of T_N and gets amplified into the collector current of T_N which in turn raise the base of T_P. This base voltage in turn gets amplified at its collector and drives the base of T_N. This way, when transistor T_N starts conducting both transistors drive one another rapidly into saturation resulting in a regenerative switching action. This rapid action changes the anode current I_A into a value determined by the load resistor and the applied voltage.

Turn off is accomplished by opening the gate, maintaining V_{AA} into a constant voltage and by increasing the load resistor R_L so as to reduce the anode-cathode current to the holding current of the SCR. For a typical SCR the holding current I_H is around 5 ma. When I_A is made equal to I_{AC}, there is sufficient current to maintain both the transistors in saturation. When one of the transistors comes out of saturation, each drives the other rapidly into cut-off. This makes the SCR switch to go in its stable *off* state.

Objective

To study the various aspects of SCRs.

Experimental Set Up

Equipments needed

1. VTVM—1 No.
2. Milliammeter — 1 No.
3. CRO—1 No.
4. Filament Transformer 230/6.3V—1 No.
5. Power supply 30 V/1 A—1 No.

Components required

1. SCR SN 101 or equivalent—1 No.
2. Resistor 100 ohms 10% 2 W—1 No.
3. Toggle switch DPDT—1 No.
4. Resistors 1 k. ohm, 10 k. ohms, 3.3 k. ohms, 10% $\frac{1}{2}$ W—1 No. each.
5. Resistor 1 mega ohm 10% $\frac{1}{2}$ W—1 No.

Procedure

Rig up the circuit as shown in Fig. 39.4. Voltage V_{AA} is increased from zero and watch the anode-cathode voltage V_{AC} on the CRO and the gate current I_G in the milliameter. The highest value of I_G is observed when V_{AC} goes from off to on and this is called gate triggering current I_{GT}. SCR chosen being SN 101, the V_{BO} is 100 volts. Forward voltage drop at the forward current of 1 ampere is 1.5 volt typical. The gate triggering current is 1 ma typical. The reverse gate voltage is 1 volt typical.

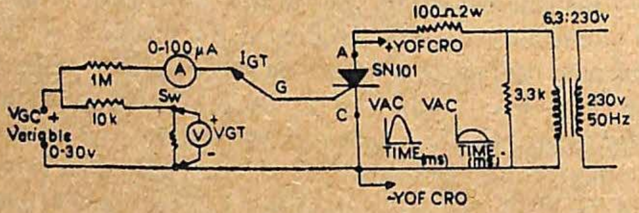


Fig. 39.4

Vary the voltage V_{GC}, measure the gate triggering voltage V_{GC} and the gate current I_G just at the moment SCR goes from *off* to *on* condition. Repeat the experiment for different values of V_{GT} within 20 per cent of its typical value. Draw the gate characteristic current V_G verses I_G.

Anode characteristics

Figure 39.4 is modified and is redrawn as shown in Fig. 39.5 to display anode to cathode characteristics. Resistors R_1 and R_{GC} divide the sweep voltage by 10. Since the triggering voltage is

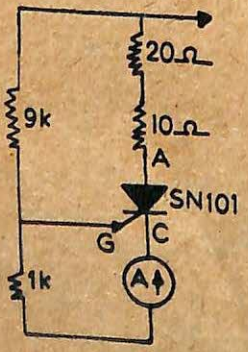


Fig. 39.5 (a)

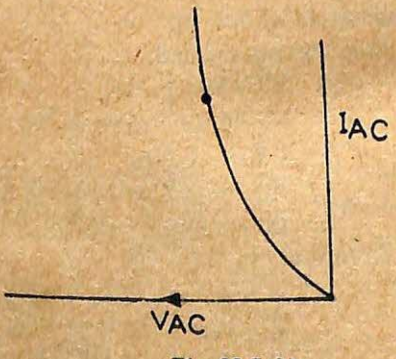


Fig. 39.5 (b)

around 0.5 V, the gate will trigger the SCR into conduction when the sweep voltage rises to 5 V. When the SCR goes into conduction measure the anode current. By varying the potentiometer R_1 the firing angle of gate is varied. Draw the anode characteristic as shown in Fig. 39.5 (b).

Fullwave Power Control

SCRs can gainfully be used in power control applications. An UJT can be used for riggering the SCR. The firing angle is adjustable using the potentiometer as shown in Fig. 39.6.

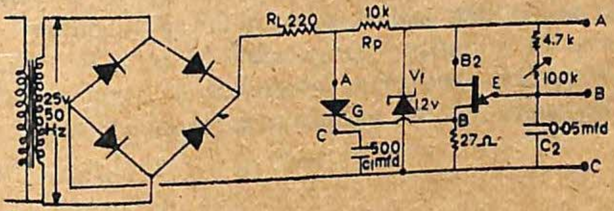


Fig. 39.6

Experimental Set Up

Equipments needed

1. Transformer 330/25V—1 No.
2. CRO—1 No.
3. VTVM—1 No.

Components required

1. Diode BY 127 or equivalent—4 Nos.
2. SCR SN 101 or equivalent—1 No.
3. Zener diode CZ 12V or equivalent—1 No.
4. UJT or equivalent—1 No.
5. Resistors 10 k. ohms, 100 k. ohms 10% ¼ W—1 No. each.
6. 27 ohms, 4.7 k. ohms 10% ¼ W—1 No. each.
7. 220 ohms 10% 2 W—1 No.
8. Capacitors 0.05 mfd (polyster)—1 No.

Procedure

Rig up the circuit as shown in Fig. 39.6. The zener diode and resistor R_P protect the UJT from excessive voltage. Capacitor C_2 and potentiometer R_E phase control of the firing angle. The SCR is triggered by the pulse generated by the UJT circuit which is connected to the gate of SCR. Depending upon the position of R_E the firing angle is varied and the power through the SCR is also varied. When the firing of the SCR takes place timing circuit gets short circuited. Measure the voltage across C_1. Vary the load R_L and measure the voltage which will give the regulation of d-c voltage. Measure ripple across the output terminal using CRO. Vary the firing angle by varying the potentiometer R_E and note the output voltage and ripple voltage.

Review Questions

1. How much voltage appeares across the SCR when it is in *on* condition and when it is in the *off* condition ?
2. Plot the volt-ampere characteristic of the SCR.
3. Why are in germanium controlled rectifiers not found in any semi-conductor manufacturer's product line?

40

DC TO AC INVERTER

Theory

The transistor d-c to a-c inverters are widely used in electronic circuitry by replacing many rotating machine converters and vibrator-transformer-rectifier converters, etc. It has the advantage of no moving part and also has higher efficiencies for small-power applications. The basic circuit of a single transformer converter is shown in Fig. 40.1. It is a simple push-pull, square wave oscillator with positive feedback from a transformer. The transistors operate as switches and maximum efficiency is got by operating them at the cut-off. Hence little power dissipation and

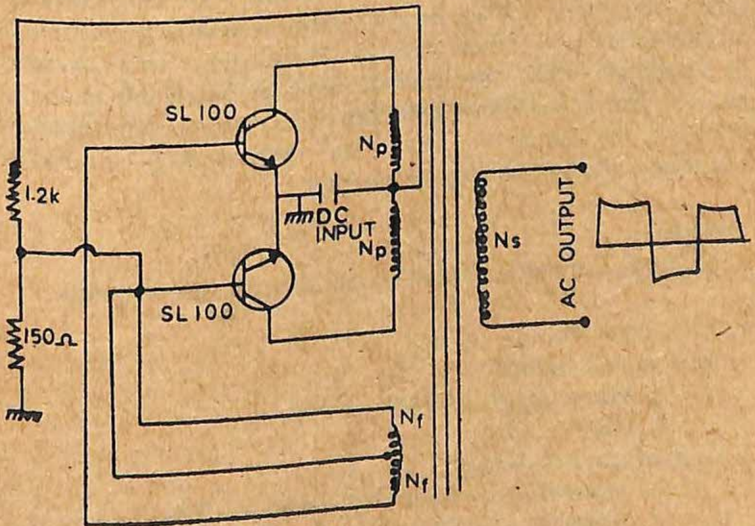


Fig. 40.1

rapid switching rate are achieved. The operating frequency requirement depends on the a-c output. The frequency response of the transistor chosen should have a ratio of 10:1 to the required frequency in order to give a trouble-free operation. Normally the circuit will self oscillate due to the positive feedback. However, when the circuit is fully loaded, the inverter may not pick up oscillation when power is connected. To overcome this incovenience a small biasing arrangement is provided using either resistors or resistor and diode. Power requirement of these transistors is very less as compared to the total power output. Generally a power rating of say, 20% of the total power output is sufficient for the transistor. The current rating of the transistor should be sufficiently higher than the load current.

The switching action of the transistors takes the magnetic core through its square loop saturation characteristics which causes the flux to change and hence voltage variation with time. The core plays a very important role in increasing the efficiency and improving the shape of output waveform. Because of the magnetic property of the core, and low rise time, there are spikes developed in the output, resulting in a large magnitude of voltage for a very short duration. These spikes are much more in amplitude when the inverter used to drive any motor or inductive loads. To some extent the spikes can be suppressed by selecting the cores like 'deltamax', 'perimander', etc., and by resulting to bifilar winding of the cores.

Objective

To study the characteristics of d-c to a-c inverter circuits.

Experimental Set Up

Equipments needed

1. Power supply 30V/2A—1 No
2. CRO—1 No.

Components required

1. Transistor SL 100 or equivalent—2 Nos.
2. Resistors 150 ohms, 1.2 kilo ohms 10% 2W —1 No. each.
3. Magnetic core CEL type T 45 or T 40—1 No.
4. Enamelled copper wire SWG 22 and SWG 30—some quantity.

Procedure

Rig up the circuit as shown in Fig. 40.1. Feed the power to the circuit. Now the transistor should go into oscillation. If the oscillation does not take place see if the windings are connected properly. If necessary, reconnect the feedback to get oscillation. The circuit is designed to oscillate at 400 Hz. When the oscillation takes place a 400 Hz noise will be audible. See the waveform of the oscillation in a CRO by connecting the probe to the collector of one of the transistors. See the base waveform also. Measure the amplitude of the secondary output. Load the circuit to the required (designed) level and observe the waveform in CRO. Switch off the power supply, with the load connected, switch on the power supply and see if the circuit oscillates. If the oscillation does not take place, vary the value of the resistors in the circuit to a lower value keeping the ratio same. Connect an inductive load and see how much spike content increases.

Review Questions

1. Discuss how the square loop characteristics of the magnetic core affects the performance of the circuit.
2. What are the reasons for the transistor cut-off frequency being higher than the oscillation frequency?
3. What are the factors determining the efficiency of the circuit?

41

RAMP GENERATOR

Theory

Ramp generators are widely used in radar circuitry, time-base circuits of oscilloscopes and in some types of digital voltmeters. It is very important to produce a ramp of a highly linear voltage because the accuracy of the instruments depends upon the linearity of the ramp. There are different methods of defining a circuit to produce a ramp waveform. For example, a ramp can be produced by charging a capacitor through a constant current source or using an integrating amplifier. Yet another device used for such purposes is the bootstrap circuit as shown in Fig. 41.1. The capacitor C_1 gets charged exponentially through the resistors R_1 and R_2 as the charging takes place, the potential at C becomes more and more positive. This causes a similar change at D from which it is coupled back to the junction of R_1 and R_2. Since the potential at D follows that at C, the potential difference across R_2 and the current through it remains

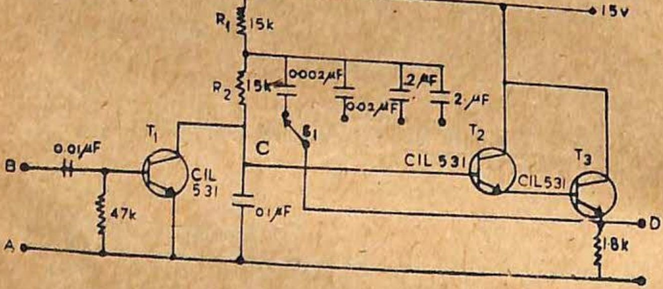


Fig. 41.1

constant. Hence the charging of the capacitor C_1 is more or less through a constant current course.

Objective

To study the properties of ramp generator.

Experimental Set Up

Equipments needed

1. Audio squarewave generator—1 No.
2. Power Supply 30V/1A—1 No.
3. Oscilloscope—1 No.

Components required

1. Transistors CIL 531 or equivalent—2 Nos.
2. Transistor 2N 3053 or equivalent—1 No.
3. Resistors 1.8 k. ohms, 47 k. ohms 10% ¼ W—1 No. each
4. Resistor 15 k. ohms 10% ¼ W—2 Nos.
5. Capacitors 0.002, 0.01, 0.02, 0.1 and 0.2 mfd (Polyster)—1 No. each
6. DPDT Switch—1 No.

Procedure

Connect the audio squarewave generator between points A and B of the circuit as shown in Fig. 41.1 and observe the waveform between A and D using an oscilloscope. The transistor T_1 is momentarily turned on by the positive going edge of the waveform at D. The capacitor C_1 is shunted by T_2. Momentarily capacitor C_1 is discharged. Then adjust the frequency of the oscillator until the stationary pattern of the ramp voltage is obtained. Switch S_1 is used to vary the feedback of the emitter follower and that S_2 to select either single or multiple emitter follower. The switch S_1 can be used to vary the feedback to the emitter follower. Vary the position of the switch S_1 for different feedback and observe the waveforms displayed in the CRO. Estimate the linearity of the ramp from the observation made in the CRO.

Review Questions

1. What factors determine the linearity of the ramp ?
2. How the frequency limitations of the transistor affects the ramp?

42

DIODE CLIPPERS

Theory

Diodes are used as clippers widely in electronic circuitry. Clippers are frequently biased to effect limited action at specific levels. A conventional junction diode will clip only one peak of the input voltage. The clipping can be either for the positive or the negative voltage. When the applied voltage is insufficient to drive a diode into the conducting state, the diode acts as variable resistor in an RC circuit. Low amplitude waveforms will not be clipped, but they will be altered by the RC properties of the diode. Reverse bias in a diode clipper raises input voltage at which conduction occurs. It is important to observe whether the biasing voltage provides forward or reverse bias to the diode. The voltage experienced by the diode is the algebraic difference of the input and the biasing voltages. Clipper circuits are designed with diodes in series, in parallel and in series-parallel combinations. Such diode networks, with special biasing conditions, appear in computer, comparators, voltage regulators and in many other applications. Basic principle of diode clippers are investigated in this experiment.

Objective

To understand the applications of diode in clipper circuits.

Experimental Set Up

Equipments needed

1. Function generator—1 No.
2. Power supply 30V/1A—1 No.
3. CRO—1 No.

Components required

1. Diode—1 No.
2. Resistor—1 No.

Procedure

Choose a diode of suitable voltage and current ratings. Rig up the circuit as shown in Fig. 42.1 with a suitable value of *R* to limit the diode current to a safe level. Connect a function generator to the input side. Bias the circuit using a variable power supply as shown in the figure. Give a sinusoidal input of frequency appropriate to the diode chosen. See the output wave-form in a CRO. Vary the bias condition and repeat the experiment. Give a square wave input and observe the results. Clipping action of diodes for circuits, shown in Figs. 42.2 to 42.4, can be observed in the same manner mentioned above.

Draw the waveforms in a graph sheet.

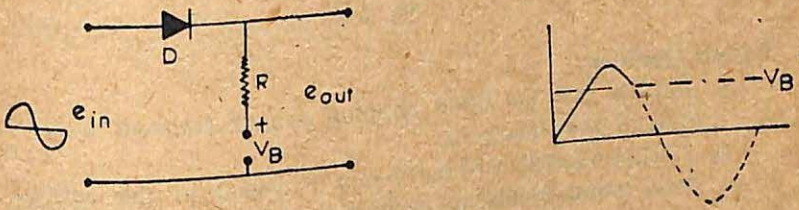


Fig. 42.1

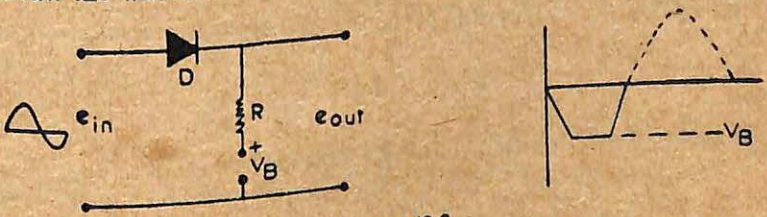


Fig. 42.2

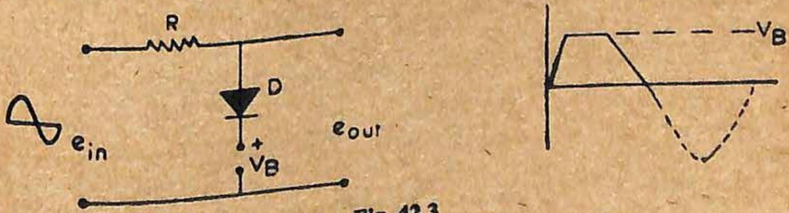


Fig. 42.3

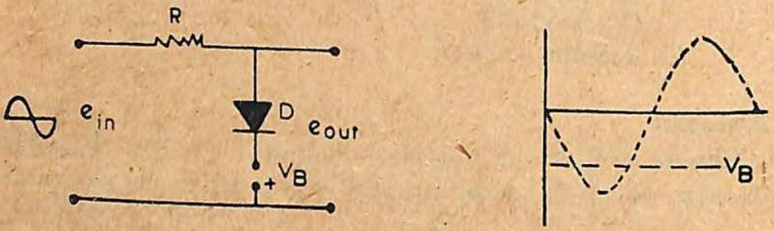


Fig. 42.4

Review Questions

1. Explain how the diode clipping circuits transmit only a part of the waveform.
2. Design a circuit which will clip the signal to the desired level symmetrically on both sides of the zero axis.

43

DIODE CLAMPERS

Theory

In electronic circuits, there are many occasions in which the d-c level of a signal has to be changed from its existing level to suit the operation of some other circuits. This operation is achieved using clamping circuits. There are many such clamping circuits using large number of components. In this experiment, simple diode clamping circuits are chosen for demonstrating the principle of clamping. When a signal is passed with diode in parallel condition, the level of the signal gets altered depending upon the other circuit parameters. A silicon diode requires a minimum of 0.5 to 0.7 volt for going into conduction whereas a germanium diode needs only 0.1 to 0.2 volt. The frequency limitations of the diode play an important role in handling the input signal.

Objective

To study the diode clamping circuits in various configurations by feeding a sinusoidal input signal of suitable amplitude.

Experimental Set Up

Equipments needed

1. Audio oscillator—1 No.
2. CRO—1 No.
3. Power supply 30 V/1A—1 No.

Components required

1. Diode CA 57 or equivalent—1 No.

2. Resistor 10 k. ohms 10% $\frac{1}{4}$ W—1 No.
3. Resistor 33 k. ohms 10% $\frac{1}{4}$ W—1 No.
4. Capacitor (polyster) 0.1 mfd—1 No.

Procedure

Rig up the circuit one by one as shown in Fig. 43.1 to 43.4. Feed a signal of frequency 1 kHz and an amplitude of, say, 10V_{pp} to the input. Observe the waveform of the output in a CRO. Carefully monitor the d-c shift in the signal conditon in the CRO. Vary the amplitude and frequency of the input and

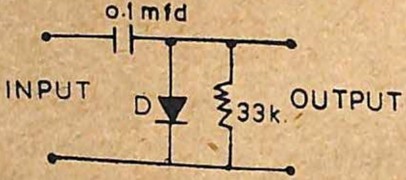


Fig. 43.1

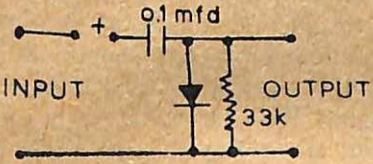


Fig. 43.2

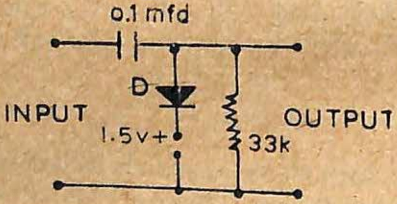


Fig. 43.3

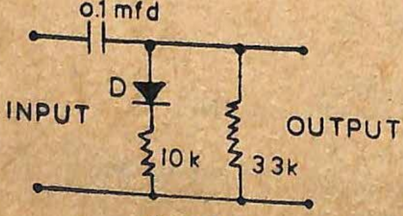


Fig. 43.4

repeat the experiment. Keeping the input voltage at $1V_{pp}$, repeat the experiment and sketch the waveforms.

Review Questions

1. Sketch the output for an input of $10V_{pp}$ theoretically.
2. How would the clamping circuits respond to sudden changes for the input signal level when shunting resistor across the diode is removed ?

44

TRANSISTOR SWITCHING

Theory

Large current characteristics of common-emitter transistor configuration were studied in the transistor characteristics experiment. Any steep change in the base-emitter bias results in similar changes in the collector current. The inter-electrode capacitance of the transistor and other stray capacitances affect the wave shaping characteristics of the transistor circuit, besides other characteristics of the transistor. The technical data of any transistor will give the following information like alpha (α) cut off frequency and in certain cases the switching characteristics. The alpha cutoff frequency gives the information on the highest possible operating frequency. The switching characteristics are referred generally as delay time, rise time, storage time and fall time. These 'times' give the proper perspective into the working of characteristics.

Delay time is the time interval required for the collector current to rise to 10 per cent of the maximum current starting from zero.

Rise time is that for collector current to rise from 10 to 90 per cent of the maximum current.

Storage time is the interval from the instant on signal switches to off signal, to the instant the collector current actually begins to fall towards cutoff.

Fall time is the time interval during which collector current decreases from 90 to 10 per cent of its maximum value.

With a known square wave input, it is possible to observe the switching characteristics in a CRO. Transistors used in high speed switching circuits such as computers, the characteristics are very important for the reliability of the machine.

Objective

To observe the effects transistor switching parameters on square waves.

Experimental Set Up

Equipments needed

1. CRO—1 No.
2. Power supply 30 V/1A—2 Nos.
3. Square wave generator—1 No.

Components required

1. Transistor CIL 769 or 2N 2369 or equivalent—1 No.
2. Resistor 100 ohms 10% $\frac{1}{2}$W—1 No.
3. Resistor 270 ohms 10% $\frac{1}{2}$ W—1 No.
4. Resistor 20 k. ohms 10% $\frac{1}{2}$W—1 No.

Procedure

Rig up circuit as shown in Fig. 44.1. Give an input square wave of 1 kHz PRF, 1 milli second duration. Observe the values of rise time T_R, storage time T_S and fall time T_F of the input waveform using a CRO. Observe the output signal in the CRO with expanded vertical and horizontal scales as far as possible and setting the brightness of the trace to the maximum. Find out the T_R, T_S and T_F of the output waveform. Feed squared pulses and observe the trace of the input waveforms and tabulate.

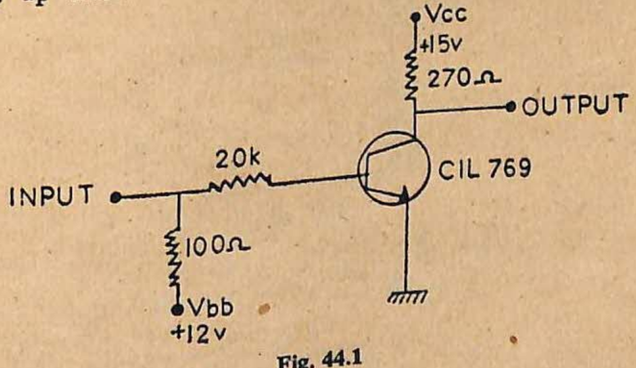


Fig. 44.1

Vary the input amplitude to saturation level in steps and observe the output amplitude, T_R, T_S, pulse duration T_D (time between 90 per cent, points) for each of the settings. Adjust the input signal amplitude to near saturation level and observe the output amplitude. Then, maintaining constant output amplitude, vary the input PRF to the highest possible PRF of the generator and observe the distortion of the output waveform with respect to the increase in the PRF. Change the value of R_L so that the peak collector current will be only 10 per cent of the maximum allowable current. Find out the storage time for low collector current as against that for high collector current.

Review Questions

1. What is the maximum switching gain that is $\frac{I_{c\,sat}}{I_b}$ for the transistor used ?
2. When the transistor acts as a saturated switch, what is the collector-base voltage ?

45

DIODE RESISTOR LOGIC CIRCUITS

Theory

Logic circuits play a very important role in electronics. With a wide range of logic circuits, many events can be made to operate. Functions like *AND* and *OR* functions can be developed using diodes and resistors. In order to illustrate *AND* and *OR* logics, the following example will suffice. In the Fig. 45.1, two switches are in series with the energising coil of a relay. When *A* and *B* are closed, the coil gets energised. This illustrates the *AND* function. In the Fig. 45.2, the coil gets

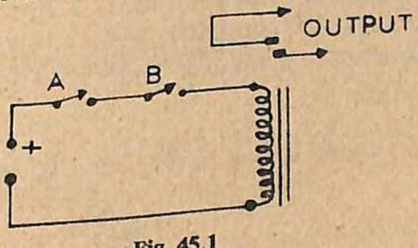


Fig. 45.1

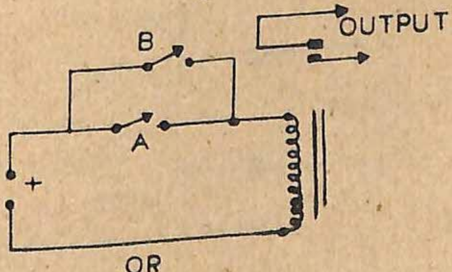


Fig. 45.2

energised when either *A* or *B* switch is closed. This illustrates for *OR* circuit.

The above mentioned logic functions can be designed using diodes and resistors. In this circuit, the *on* or *off* condition is denoted as binary level 1 or 0. When the binary level is 1, the output shown will be, say, 6 volts. When the binary condition is shown as zero, the output will be zero volt. It makes no difference, what voltages are used to represent the logical one and zero. All that is important is the level.

Objective

To determine the operation of diode resistor *AND—OR* circuits.

Experimental Set Up

Equipments needed

1. Power supply 30V/1A—3 Nos.
2. VTVM—1 No.

Components required

1. Diodes CD 31 or equivalent—6 Nos.
2. Resistor 470 ohms 10% ¼W—2 Nos.
3. Resistor 10 k. ohms 10% ¼W—2 Nos.

Procedure

The *AND* circuit shown in Fig. 45.3 is wired. Observe the output as per the truth table shown in Table 1. This circuit has 2 inputs leads which may be separately connected either to zero or 6 volts. The truth table can be completed by connecting the inputs suitably. Similarly for the Fig. 45.4, follow the same

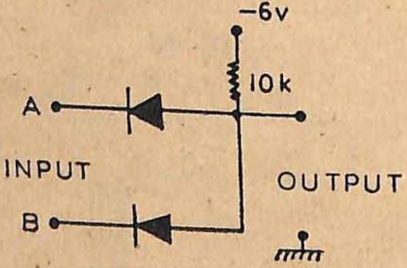


Fig. 45.3

TABLE 1

Input volts	Output volts
A	B
0	0
0	+6
+6	0
+6	+6

TABLE 2

Input volts	Output volts
A	B
0	0
0	+6
+6	0
+6	+6

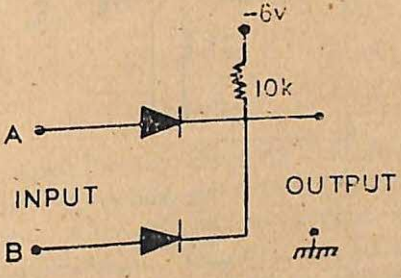


Fig. 45.4

procedure and complete the truth Table 2. This will explain the *OR* circuit.

The Fig. 45.5 is also is a combinational circuit. In this three inputs can be given. Fig. 45.6 is also is a combinational circuit, the truth table for which is given in Table 3. Feed the signal as per the truth table and observe the output voltages and tabulate accordingly.

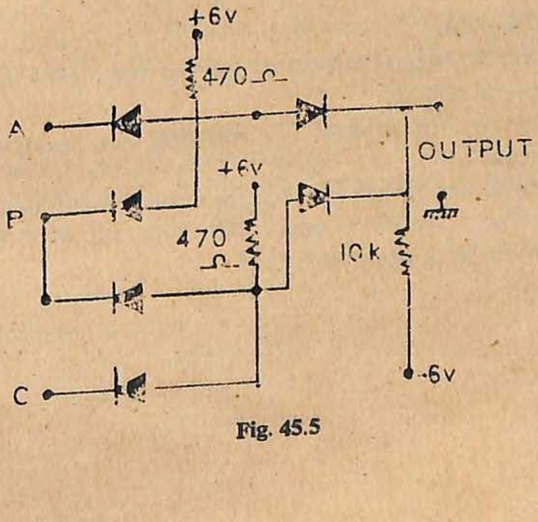


Fig. 45.5

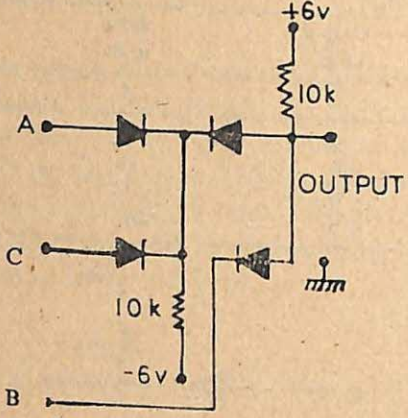


Fig. 45.6

TABLE 3

Input volts			*Output volts*	
A	*B*	*C*	*Fig. 45.5*	*Fig. 45.6*
0	0	0		
0	0	+6		
0	+6	0		
0	+6	+6		
+6	0	0		
+6	0	+6		
+6	+6	0		
+6	+6	+6		

Review Questions

1. Write the logical expression for the output of the combinational circuits.
2. What are the criteria for selecting the resistance in the circuits ?
3. Analyse the circuit for the case of equal resistance levels.
4. What is a negative logic ? Construct an *AND* and *OR* circuits for a negative logic ?

46

TRANSISTOR LOGIC CIRCUITS

Theory

The diode resistor logic circuits have a disadvantage that they get quickly loaded down. To overcome this defect, transistors are used in the design of the logic circuits. The nature of the common-emitter transistor circuits is such that when the base voltage of the transistor is increased, the collector voltage decreases for an *npn* device. This phenomenon gives an inversion property. This is called as complementation of a variable also. A small base current controls a relatively large collector current. Therefore a transistor logic circuit can drive many subsequent stages of similar types. The transistor logic gate always results in a circuit that provides an inversion of *AND* or *OR*, which are generally termed as *NAND* and *NOR* logic operations. These two combinations can be used in different ways to derive the needed *AND*, *OR* and other logics. The various circuits can operate either on positive or negative logics. For the experiment a positive logic is chosen.

Objective

To study the circuit operation of a diode transistor logic circuit for *NAND* and *NOR* logics. Also to determine the fan-out capability of the circuit.

Experimental Set Up

Equipments needed

1. Power supply 3 V/1A—2 Nos.
2. VTVM—1 No.

Components required

1. Transistor CIL 531 or equivalent—2 Nos.
2. Diode *CD* 31 or equivalent—2 Nos.
3. Resistor 2.2 k. ohms 10% $\frac{1}{4}$W—1 No.
4. Resistor 100 k. ohms 10% $\frac{1}{4}$W—2 Nos.
5. Potentiometer (wire wound) 5 k. ohms 2W—1 No.

Procedure

Rig up the circuit as shown in Fig. 46.1. Draw the truth table as shown in Table 1, and note the output voltages for various input conditions as laid down in the Table. Repeat the experiment for other two circuits and enter the readings against Tables 2 and 3 respectively. An important point, that has to be

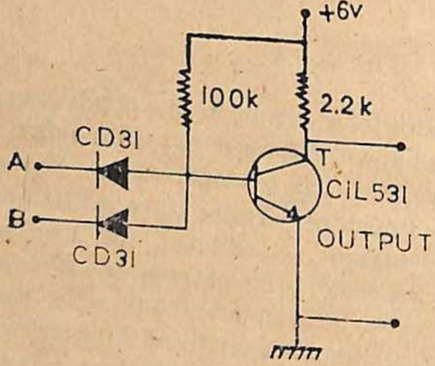


Fig. 46.1

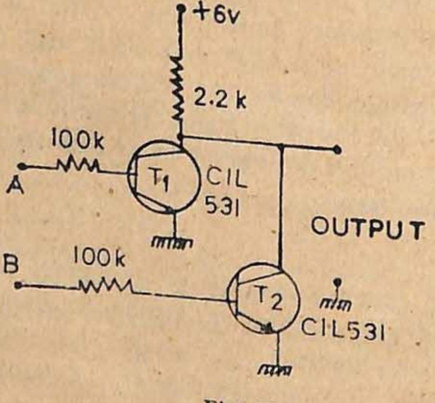


Fig. 46.2

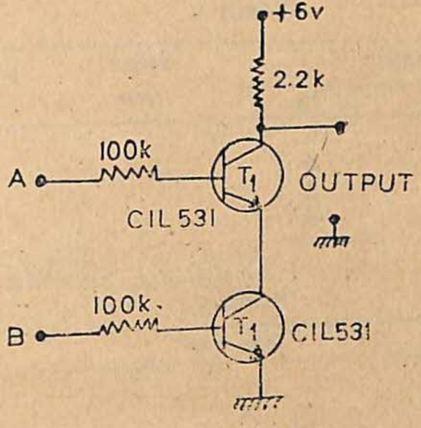


Fig. 46.3

kept in mind is that the supply voltages should be set accurately as in the figure. In addition, determine the value of the load resistance that brings the transistor out of saturation. This can be determined using, say, a 5 k. ohms potentiometer as load and slowly reducing its value while monitoring the collector voltage. The value of the resistance which starts bringing the output voltage from its low saturation value is entered in Table 4 for each of the circuits. Before doing this experiment, it should be noted that the input to each of the circuit should be such that a transistor in each case is in perfect saturation before the potentiometer was connected.

TABLE 1

Input volts		Output volts	V_{ce}
V_A	V_B		
0	0		
0	6		
6	0		
6	6		

TABLE 2

Input volts		Output volts	V_{ce_1}	V_{ce_2}
V_A	V_B			
0	0			
0	6			
6	0			
6	6			

TABLE 3

Input volts		*Output volts*	V_{ce_1}	V_{ce_2}
V_A	V_B			
0	0			
0	6			
6	0			
6	6			

TABLE 4

Figure	*Min. load*	*Resistance*
Fig. 46.1	...	ohms
Fig. 46.2	...	ohms
Fig. 46.3	...	ohms

Review Questions

1. Analyse the circuit and explain how they work in terms of voltages and currents for various input conditions.
2. Draw a similar circuit to that of the one shown in Fig. 46.1 for three input conditions.
3. Equate the minimum value of load resistance which each circuit can drive.

47

LINEAR SWEEP CIRCUIT

Theory

A linear sweep voltage may be generated by charging a capacitor from a constant-current source. The linearity of the waveform is very much better than that produced by charging a capacitor exponentially through a resistor. In the case of capacitor-resistor sweep generator the wave amplitude of the voltage is small compared to the source voltage. This disadvantage is overcome if a constant current source is used to charge the capacitor. A good example of a constant current-source is a transistor employed in a grounded base configuration with a zener diode connected as shown in the Fig. 47.1.

The collector current in this grounded base configuration is approximately equal to the emitter current regardless of the value of load resistor. The emitter current is held constant by the voltage drop across the zener diode and the emitter resistor. Even when there is a fairly big fluctuation in the voltage at the emitter, zener can take care of the fluctuation and present a constant voltage across it. This in turn maintains a constant current in the circuit. The capacitor C is charged through the constant current source consists of transistor T_1, zener diode, resistor R_E, etc. Once the transistor is charged it has to be discharged. This can be done using a switch. Transistor T_2 act as a switch which closes during the duration the input voltage is in the positive level. When the input voltage is positive the transistor T_2 gets forward bias and hence starts conduction. When this transistor conducts the emitter-collector region acts as a short and the capacitor gets discharged. During the period for which the amplitude of the input is negative the transistor T_2 is cut off and capacitor gets charged to the level of V_{CC}. This action of charging and discharging takes place depending upon the duration of the input waveform.

Objective

To study the sweep circuit using a constant current source.

Experimental Set Up

Equipments needed

1. CRO—1 No.
2. Pulse Generator—1 No.
3. Multimeter—1 No.
4. Power supply 30V/1A—2 Nos.

Components required

1. Transistor CIL 531 or equivalent—1 No.
2. Transistor CIL 769 or equivalent—1 No.
3. Zener Diode CZ 4.7 or equivalent—1 No.
4. Resistors 4.7 k. ohms 6.8 k. ohms, 10 k. ohms 10% ¼W—1 No. each
5. Capacitor 0.1 mfd (Polyster)—1 No.

Procedure

Rig up the circuit as shown in Fig. 47.1. Keep the V_{CC} and

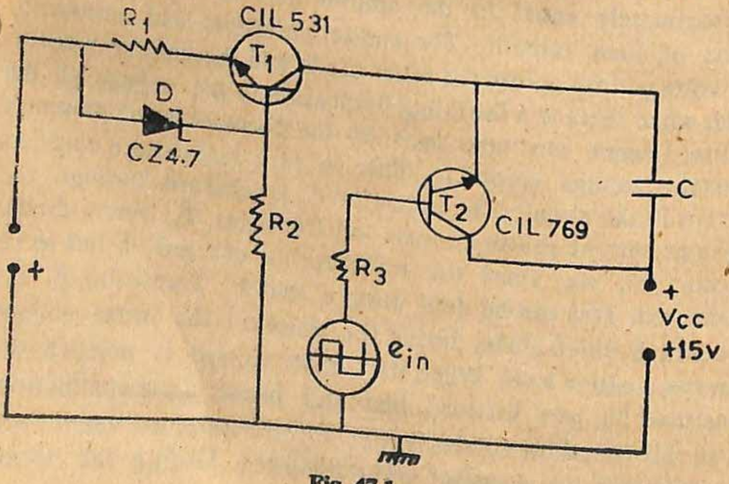


Fig. 47.1

V_{EE} at 10 volts. Connect the multimeter to the emitter of T_1 and see the amount of current flowing into the circuit with power supplies on. Connect the pulse generator to the base of T_2 and suitably adjust the PRF and the pulse duration. See the sweep waveform in a CRO across the capacitor. Vary the PRF and pulse duration and repeat the experiment.

Review Questions

1. On what does the sweep speed depend?
2. What is the amplitude of the input to trigger T_2?

48

UNIJUNCTION TRANSISTOR

Theory

The unijunction transistor possesses a negative resistance characteristic which comes in handy in the construction of oscillator, timing circuits, trigger circuits, etc. A typical UJT is shown in Fig. 48.1. An oscillator using UJT requires only very few components as compared to conventional circuits. The operation of the UJT can be explained using the diode resistor model of the device as shown in Fig. 48.2. When there is no voltage applied to the emitter, the voltage at the cathode end of the emitter base diode is determined by V_{bb}, P_{b_1} and R_{b_1} potential divider circuits. At this point the diode will be reverse biased and only very small emitter current will flow. When a voltage V_{ee} is applied to the emitter circuit, still the diode will remain in the reverse biased condition until V_{ee} exceeds the voltage at the other end of the diode by about 0.6 volt. When the junction gets forward biased, a substantial current begins to flow

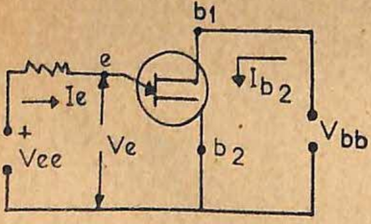


Fig. 48.1

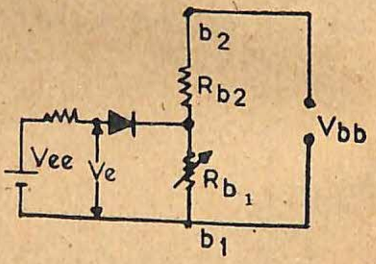


Fig. 48.2

from the emitter to the base No. 1. This current lowers the value of the resistance of the silicon bar shown as P_{b_1}. The voltage V_{ee} must drop to a lower value as determined by the voltage division along the silicon bar. This means that the emitter current increases as the emitter voltage reduces and this phenomenon causes a negative resistance region in the volt-ampere characteristics of the diode.

Objective

To study the operation of UJT and use it as a relaxation oscillator.

Experimental Set Up

Equipments needed

1. Power supply 30V/1A—1 No.
2. VTVM—1 No.
3. Microammeter—1 No.
4. CRO—1 No.

Components required

1. UJT 2N 2647 or equivalent—1 No.
2. Resistor 22 ohms 10% $\frac{1}{4}$ W—1 No.
3. Resistor 270 ohms 10% $\frac{1}{4}$ W—1 No.
4. Resistor 100 k. ohms 10% $\frac{1}{4}$ W—1 No.
5. Potentiometer (linear) 100 k. ohms—1 No.
6. Capacitor (polyster) 0.05 mfd—1 No.
7. Capacitor (electrolytic) 10 mfd—1 No.

Procedure

Measure the interbase resistor of the UJT with an ohmmeter. That is by connecting the ohmmeter between the base 1 and base 2 of the device. Rig up the circuit as shown in Fig. 48.3. The

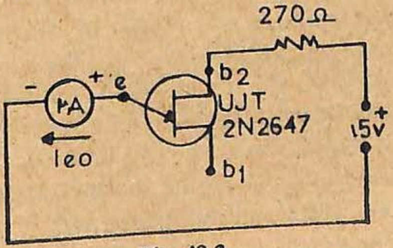


Fig. 48.3

emitter leakage current I_{eo} is measured with the base 1 open circuit condition. The leakage current of any good UJT should be very small and hence high sensitivity currentmeter should be used.

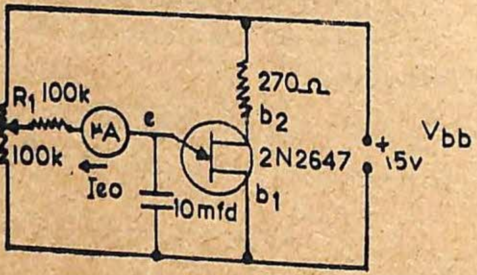


Fig. 48.4

Rewire the circuit as shown in Fig. 48.4. The peak point current I_p, emitter peak point voltage V_p and the approximate value of the valley voltage V_v are measured in the following manner. Increase the value of R_1 slowly so that the UJT fires and oscillates. When the firing takes place, there will be increase in the emitter current. The maximum value of the emitter current should be read in the meter just before the firing of UJT. This is called the peak point current. In order to verify whether the current measured was after the firing or not, following observations are to be carefully done. When the firing takes place, the currentmeter needle moves slowly. Prior to the firing, there is no such movement. Connect the VTVM in the range of 0.50 V d-c between the emitter and base point of the UJT. As the slow oscillation of the voltage occurs observe the maximum and minimum values of V_e. These readings correspond to V_p and V respectively.

Figure 48.5 is a typical circuit of a relaxation oscillator using UJT. This circuit works as a sawtooth waveform generator and also is used as a triggering circuit. Wire the circuit as shown in the figure and observe the waveform in the CRO at the emitter terminal and the base terminals. The repetitive frequency of the waveform is determined by the time constant of the resistance and capacitance connected in the emitter circuit. This value of resistor and capacitor can be varied and the frequency of the waveform may be noted.

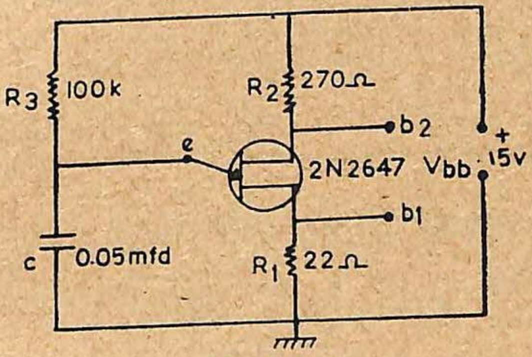


Fig. 48.5

Review Questions

1. Compare the parameters like the interbase resistance and the peak point emitter current with the values given in the data sheet.
2. Determine the frequency and the amplitude of the sawtooth output of the relaxation oscillator theoretically and compare the values with the practical readings.
3. Explain the operation of the relaxation oscillator circuit used in the experiment.

49

FIELD EFFECT TRANSISTOR

Theory

A field effect transistor is constructed from a bar of *n* or *p* type silicon material. Unlike the conventional transistor the FET has only one type of carrier. This enables the transistor to have no leakage current due to opposite carriers. The structure of a *p*-channel device is shown in Fig. 49.1. In the normal operation a current flows along the length of the channel when a voltage is applied between the source and the drain. The *n-p* junction

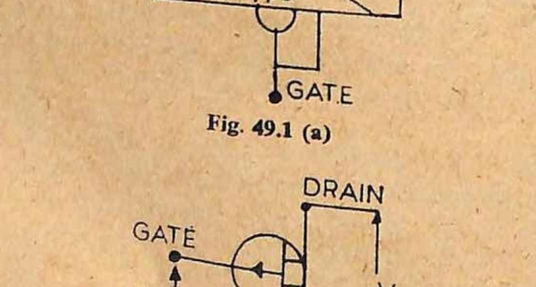


Fig. 49.1 (a)

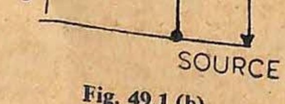


Fig. 49.1 (b)

formed by the gate material defused into the bar. As the magnitude of the reverse bias gate-source voltage is increased, the region depleted of charge is increased, and the channel becomes thinner. One of the advantages of the FET is that the gate-source junction is usually reverse biased resulting in a very small current flowing from control voltage. Hence a very high input impedance comparable to that of a vacuum tube pentode is realisable.

Objective

To study the circuit properties of FET, to obtain a set of common-source drain characteristics of the device and to use this as a low frequency voltage amplifier.

Experimental Set Up

Equipments needed

1. Power supply 30V/1A—2 Nos.
2. CRO—1 No.
3. Audio oscillator—1 No.
4. 0.5 ma d-c milliammeter—1 No.

Components required

1. FET BFW 10 or equivalent—1 No.
2. Resistor 4.7 k. ohms 10% $\frac{1}{4}$ W—1 No.
3. Resistor 27 k. ohms 10% $\frac{1}{4}$ W—1 No.
4. Resistor 220 k. ohms 10% $\frac{1}{4}$ W—1 No.
5. Resistor 1 m. ohm 10% $\frac{1}{4}$ W—1 No.
6. Potentiometer 10 k. ohms (linear)—1 No.
7. Potentiometer 100 k. ohms (linear)—1 No.
8. Capacitor (electrolytic) 10 mfd/15V—1 No.

Procedure

Wire the circuit as given in Fig. 49.2. Observe the polarities of the power source before switching on. Set the d-c drain-source voltage V_{ds} to +15 volts. Determine the value of the gate to source voltage, V_{gs}, that cuts off the transistor by adjusting the bias potentiometer 100 k. ohms. Measure the value of V_{gs}. Set the gate to source voltage at 1 volt and vary V_{ds} from 0 to 15V and obtain the corresponding drain current, I_d for each setting of V_{ds}. Tabulate these readings. The V_{ds} could be adjusted in steps of 1 volt. Repeat this experiment keeping V_{gs} potential at −0.6, −0.3, 0 and +0.5 volt and tabulate. Draw the graph connecting V_{ds} and I_d for a fixed setting of V_{gs}.

Rewire the circuit as shown in Fig. 49.3. This is a common source self biased amplifier. Record the quiescent values of V_{gs} and V_{ds}. Switch on the oscillator with the voltage of the oscillator say, 0.5 volt and frequency to 500 Hz and observe the output waveform in the CRO. Vary the input frequency, keeping the voltage constant at the input, and observe the output waveform and magnitude in the CRO and compute the voltage gain.

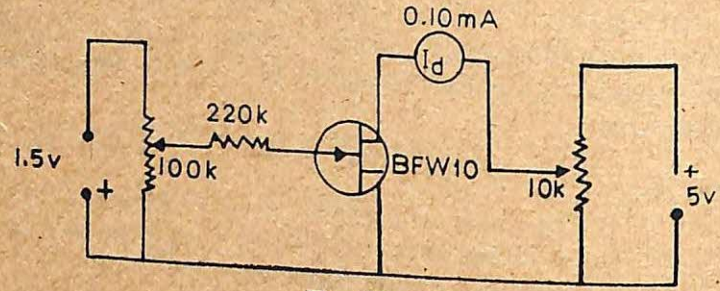


Fig. 49.2

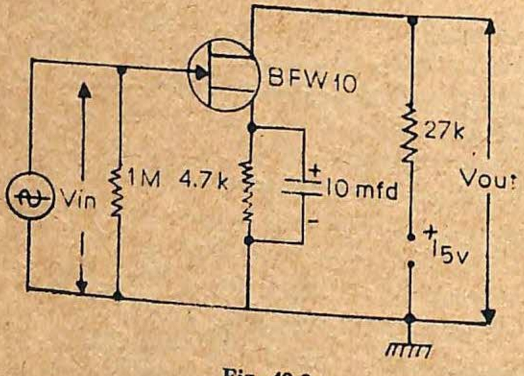


Fig. 49.3

Review Questions

1. Draw the family of common-source volt-ampere characteristics of the FET from the above experiment.
2. Determine the transconductance of the device graphically corresponding to $V_{gs} = 0$.

3. Theoretically determine the quiescent values of drain current and V_{gs} for the amplifier shown in Fig. 49.2 and 49.3.
4. Draw the circuit of a complete self biased *p*-channel FET amplifier.

50

TUNNEL DIODE CHARACTERISTICS

Theory

Tunnel diode is a widely used device wherever a negative resistance characteristic is to be stimulated in the circuit. The negative resistance characteristics can be studied through a simple experiment as explained below. The equivalent circuit of a tunnel diode as a series amplifier is shown in Fig. 50.1. In this *R* represents always the positive d-c resistance of the tunnel diode and *r* represents the variational resistance. A study of the current voltage characteristics shows that *r* is initially positive, then

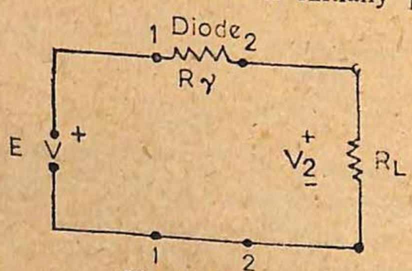


Fig. 50.1 (a)

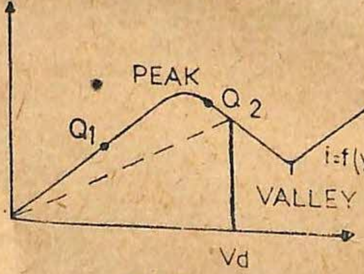


Fig. 50.1 (b)

becomes negative and again becomes positive as shown in Fig. 50.2. If the quiescent point were to be located at Q as in the curve then it is obvious that the variational resistance is in the negative region. If the Q point is located at Q_1 then both the d-c resistance and the variational resistance are positive. Thus R and load resistor R_L would provide a voltage divider. This means that for any variation in the output by *dv*, there has to be a change in the input voltage by *dE*.

Objective

To study the volt-ampere characteristics of a tunnel diode.

Experimental Set Up

Equipment needed

1. Power supply 30V/1A—1 No.
2. Multimeter—1 No.

Components required

1. Tunnel diode 1N 3712 or equivalent—1 No.
2. Resistor 4.7 k. ohms 10% $\frac{1}{4}$W—1 No.

Procedure

Rig up the circuit as shown in Fig. 50.2. Keep the voltage of the power supply to 6 volts and note the current flowing through the circuit and the voltage across the diode. Vary the supply voltage from 0 volt to say, 10 volts and note the voltage and current as mentioned above. Draw the voltampere characterstics.

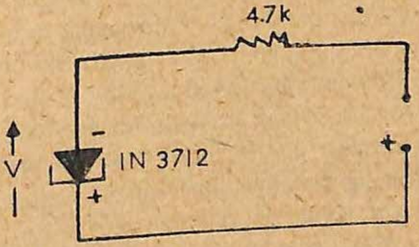


Fig. 50.2

Review Question

Explain the phenomenon of amplification using the tunnel diode.

51

IC REGULATOR

Theory

Voltage regulator Chip 723 is a monolithic device constructed using the epitaxial process. The chip contains all the basic blocks used in the design of a regulated power supply. The process of making the entire circuit out of a single chip under controlled environment ensures high performance. The temperature range to which this chip can be used is a great advantage to the designers of systems. The commercially available chips can operate from 0° C to 70° C. The military version of the same can operate from $-55°C$ to $+125°C$. Availability of the chip in dual-in-line package with 14 leads or the 10 leads metal can package comes in handy to the designer to choose the appropriate package for the circuit. The maximum power output is 800 mw and the power handling capacity of the regulator can be augumented by connecting components externally to the chip. A continuously variable power supply could be made use of, for any power rating using the chip. Some of the typical features of this regulator are line regulation 0.01 per cent of V_{out}, load regulation 0.02 per cent of V_{out} ripple rejection 74 dB and temperature coefficient of output voltage 0.002 per cent °C. The maximum input voltage that can be given is 40 volts and the maximum output voltage that can be derived is limited to 37 volts. This chip incorporates a current sensing and current limiting circuit to protect the regulator from over load and short circuit conditions.

Objective

To make a regulated power supply using an integrated circuit and study the performance.

Experimental Set Up

Equipments needed

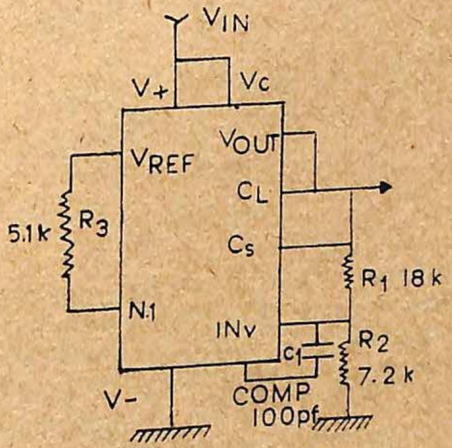
1. Unregulated power supply 40 volts d-c at 1 Ampere—1 No.
2. Digital Voltmeter—1 No.
3. CRO—1 No.

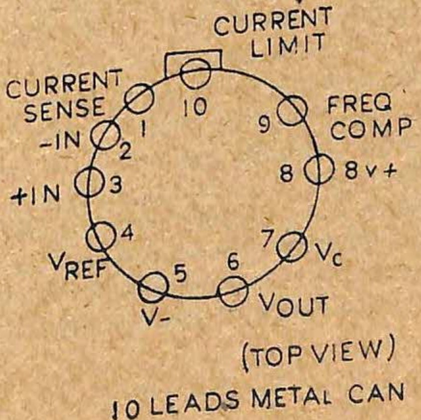
Components required

1. Regulator chip IC 723 or equivalent—1 No.
2. Resistance 5.1, 7.2, 18 k. ohms, $\frac{1}{4}$W, +5%—1 No. each
3. Capacitor (Styroflux) 100 pf, 50V—1 No.

Procedure

Rig up the circuit as shown in Fig. 51.1. Take care to see that





connections are made to the correct pin number only. Look for the sense of direction for the connection in Fig. 51.2. Connect

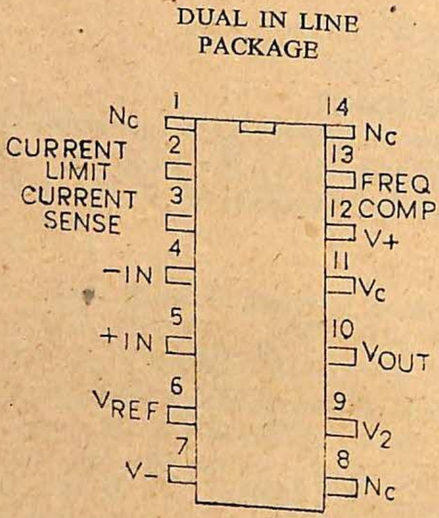


Fig. 51.2

the power source to the circuit observing the appropriate polarity. Study the characteristics of the power supply in the following manner: (i) vary the input voltage and observe the variation in the output of the regulator and calculate the percentage variation in the output for an input variation of 10 per cent over the nominal voltage. For example, if the nominal input voltage is, say, 30 volts and the output is configurated for 25 volts, observe the output variation for an input variation from 27 volts to 33 volts, (ii) connect a load to draw a current such that the total power output is less than 800 mw by using a rheostat of value, 100 ohms and slowly vary the load within the limits as calculated above and observe the fall in the output voltage. Calculate the percentage change in the output voltage to reckon the regulation, and (iii) use a CRO to observe the ripple voltage at the output for loaded and unloaded condition. Rewire the circuit as shown in Fig. 51.3 to increase the power handling capacity and repeat the experiment.

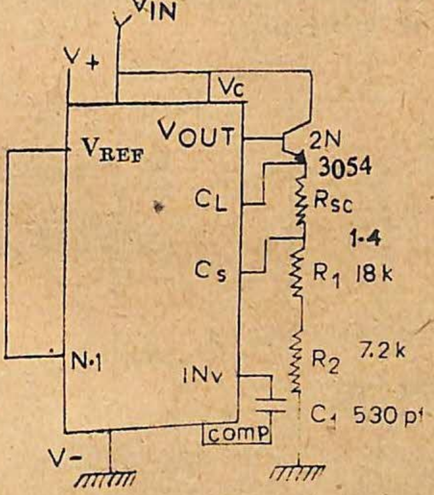


Fig. 51.3

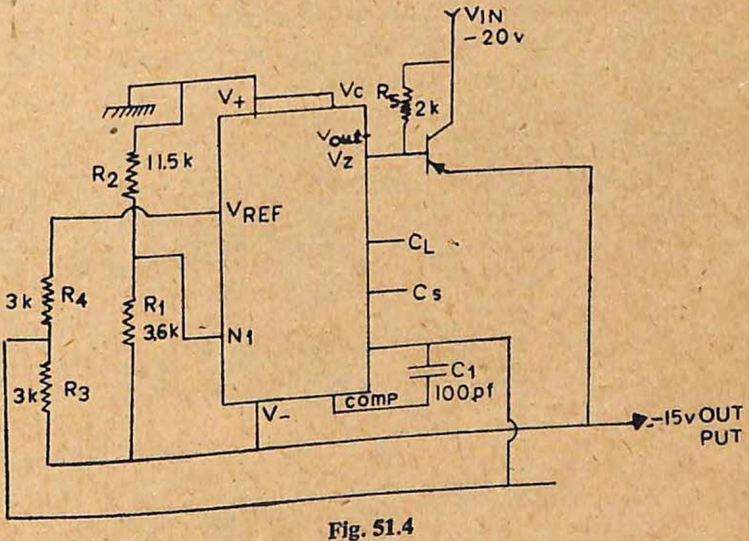


Fig. 51.4

Review Questions

1. Examine whether the chip 723 can be used as a negative voltage regulator (refer Fig. 51.4).

2. Connect the regulator chip for an output voltage of 2 to 7 to 7 volts (refer Fig. 51.5).

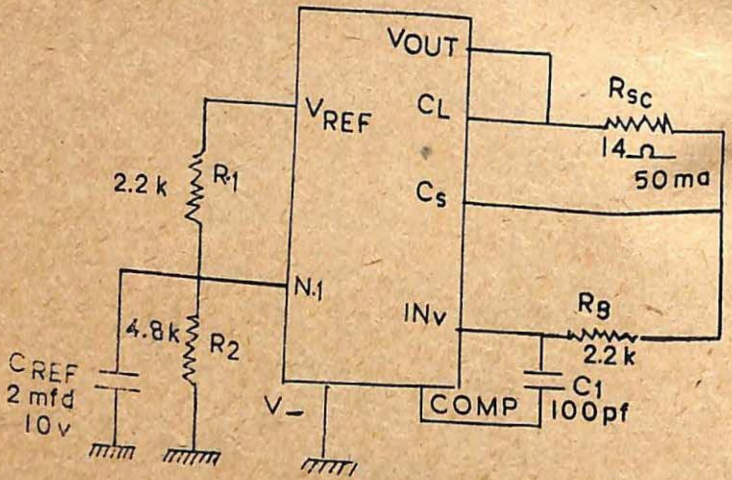


Fig. 51.5

52

IC COMPARATOR

Theory

Voltage comparators are widely used in electronic circuits as limiters, simply analog to digital convertors pulse, square and time delay generators, wide range of voltage controlled oscillators, multivibrators, etc. There are many design-committed comparators available in the market. Operational amplifiers are extensively used as comparators as they are available over a wide range of operating conditions. Among the many functions performed by comparators signal squaring and pulse detection are frequent applications in circuitry. Signal squaring is one of the simplest roles for a comparator because it only requires high gain to transform a rounded signal to sharp pulses. There are many comparators for varying speed requirements. Integrator circuit LM 311 is one such comparator.

Objective

To study the characteristics of a comparator as (i) zero crossing detector and (ii) free running multivibrator.

Experimental Set Up

Equipment needed

1. Power supply ±15 volts 100 ma—1 No.
2. CRO—1 No.

Component required

1. IC comparator LM 311 or equivalent—1 No.
2. Resistors 1, 10 and 39 k. ohms ¼W, ±5%
   —1 No. each.

3. Resistor 20 k. ohms, $\frac{1}{4}$W, ±5%—2 Nos.
4. Capacitor (Styroflux) 1200pf, 30 volts—1 No.

Procedure

Rig up the circuit as shown in Fig. 52.1. In order to enable the reuse of the IC, an IC socket may be used. The corresponding pins are brought out separately by wire and components soldered for the experiment. The circuit (Fig. 52.1) is used as zero crossing detector. As the input crosses the zero point and reaches the level of, say, +5mv output the circuit goes to one level. This level can be used to switch on or switch off a mosfet (metal oxide semiconductor FET) for further application. In this experiment, it is sufficient to detect an output corresponding to a zero input. For this, ground the input and not the output. Raise the input voltage to a level of 5 mv or more and the output goes to a + one level.

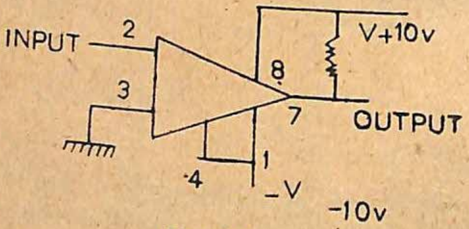


Fig. 52.1

The circuit shown in Fig. 52.2 is the circuit configuration for a 100 kHz free running multivator. Rig up the circuit as shown with the values mentioned in the diagram. This configuration should oscillate at 100 kHz rate, note the waveform. Vary the values of C_1 and note the frequency of oscillation.

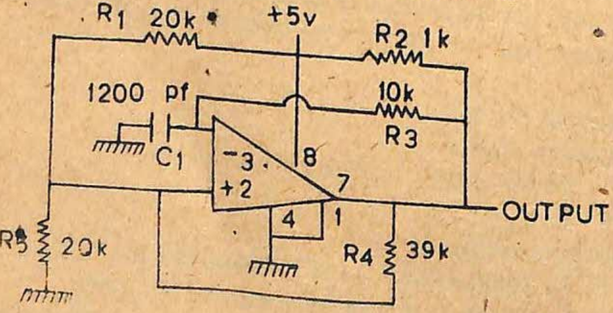


Fig. 52.2

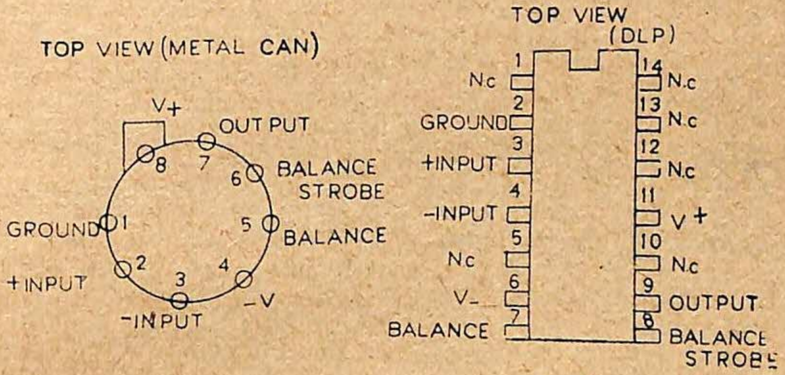


Fig. 52.3

Review Question

What are the other uses to which LM 311 can be put to ?

53

IC TIMER CIRCUIT

Theory

Timing circuits are very widely used in industrial and other equipments. The invention of timer chip LM 555 is handy in designing timer circuits. This chip produces accurate time delays which is controlled with two external resistors and a capacitor. When a trigger signal is applied, the timing cycle gets repeated. The flip-flop inside the chip is then set, immunising the circuit from any further trigger signals. To interrupt the timing cycle a reset signal is applied. When the chip is used in monostable operation, time delay can be obtained using external resistors and capacitors. Referring to Fig. 53.2, the external capacitor is initially held in discharged condition by a transistor inside the timer chip. When a negative pulse is applied to triggers the flip-flop is set and the short across the external capacitor is removed. This allows the capacitor to charge through the resistor R_1. As the voltage across the capacitor C_1 rises to 2/3 of supply voltage V_{CC}, the comparator inside the chip resets the flip-flop. When this happens the capacitor discharges rapidly and the output is driven low. The circuit triggers on a negative-going input signal when the level reaches 1/3 of the supply voltage. Once triggered, the circuit remains in this state until the set time has elapsed. The duration of the output high state is given by $t=1.1\ R_1C_1$. Since the charge rate and the threshold level are both directly proportional to supply voltage, the timing interval is independent of supply.

Objective

To use a LM 555 for a delay of 100 m sec.

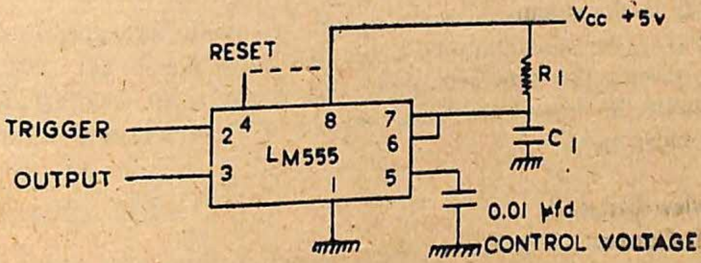


Fig. 53.1

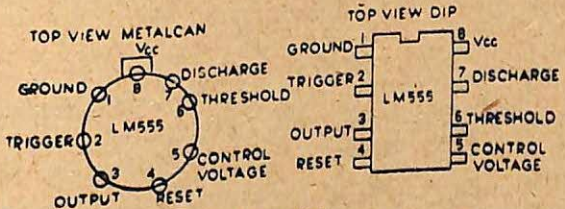


Fig. 53.2

Experimental Set Up

Equipment needed

1. Power supply 0-10 V, 100 ma and 5 V, 100 ma —1 No. each.
2. CRO or time interval unit—1 No.
3. Stopwatch—1 No.
4. Trigger source (pulse generator)—1 No.

Component required

1. Timer chip LM 555 or equivalent—1 No.
2. Resistor 1 meg ohm, 1/4W.±5%—1 No.
3. Capacitor (polyster) 0.08 and 0·01 mfd—1 No. each.

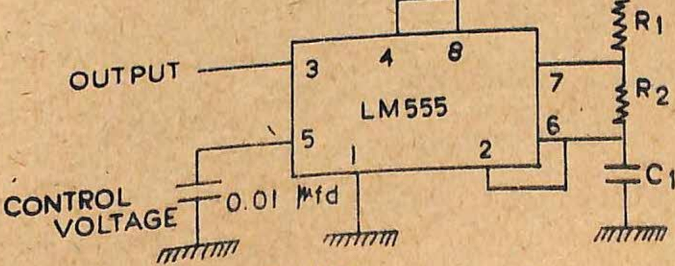


Fig. 53.3

Procedure

Rig up the circuit as shown in Fig. 53.1, with the values of R_1 and C_1 as mentioned above. Apply the trigger signal, say, 1.67V and observe the waveform across the capacitor in a CRO and compute the delay time. Vary the value of R_1 and C_1 and repeat the experiment.

Review Question

1. Convert LM 555 for a stable operation (Refer Fig. 53.3).

54

TTL GATES

Theory

Transistor-transistor logic integrated circuits are widely used in digital applications. There are many circuits available based on this technology for varied uses. The simplest among them are the NAND, NOR gates. Realisation of NAND gate means negation of AND. AND function can be considered as a lamp connected using two switches in series. Unless both the switches are 'ON' the lamp does not glow. NAND function is the negation of AND. A two input NAND gate is shown schematically in Fig. 54.1. The inputs to the TTL circuit have

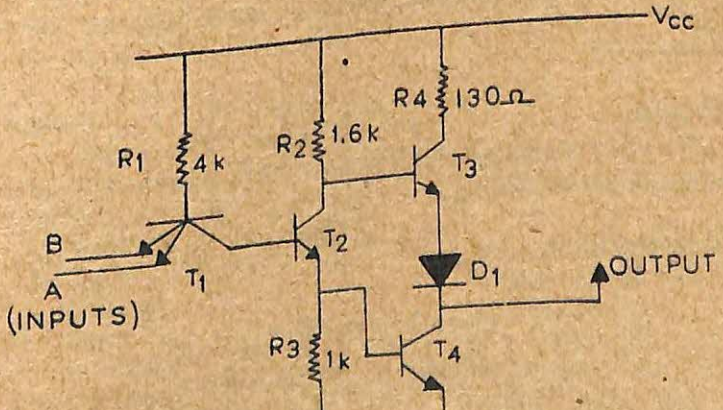


Fig. 54.1

known fixed levels. That is signal level is considered '1' if the amplitude of the signal is 2.4 volts or above but below the supply voltage V_{cc} which is 5 volts ± considered as a low level input.

Logical decisions are made in digital circuits by logic gates. A logic gate is a two-state logic element whose output is determined by its functional type and the immediate condition of its inputs. The frequently encountering terms in the logic gates are 'logic-high' and 'logic-low'—logic varying between 2.4 and 5. This state is also called as on state. The 'logic-low' is that state corresponding to voltage level in the output varying between 0 to 0.8 volts. This state is also known as off state. The five basic types of gates commonly used are NOT, NAND, AND . NOR, OR. For two inputs A and B, the following truth table shows the output conditions.

Inputs		*Outputs*				
A	B	NOT	NAND	AND	NOR	OR
0	0	1	1	0	1	0
0	1	*	1	0	0	1
1	0	*	1	0	0	1
1	1	0	0	1	0	1

*NOT gate has only one input and is often called an inverter.

NAND GATE

Objective

To study a simple NAND gate and observe its input and output logic relations.

Experimental Set Up

Equipment needed

1. Power supply+suolrs, 100 ma—1 No.
2. CRO—1 No.
3. Digital voltmeter—1 No.

Component required

1. IC SN 7400 or equivalent—1 No.
2. 14 pin socket—1 No.

Procedure

Many experiments in the logic circuit require different ICS. It is advisable to use an IC socket for plugging in the dual-in-line digital IC's. Therefore, wire up a 14 pin dual-in-line socket and bring out the connections naming 1 to 14 in the sequence shown in the diagram.

To study the NAND gate performance, plug in SN 7400 to the socket. This is a dual-input NAND gate. Refer to the truth table given below, change the level of the inputs and note the output levels corresponding to the inputs and verify truth table.

Inputs		*Outputs*
A	B	C
0	0	1
1	0	1
0	1	1
1	1	0

In order to facilitate the easy verification of the truth table using a potential divider arrangement from the same power supply feed a voltage of amplitude, say, 2.5 to 3 volts for state 1 and ground the other input point for state '0'

AND GATE

Objective

To study the operation of AND gate.

Experimental Set Up

Equipment needed : as above.

Component required : as above.

Procedure

AND is the inverse of NAND. Hence by using two NAND gates one as an inverter and the other as it is an AND gate can be made. Refer to Fig. 54.2. Connect the pins 4 and 5 together and to this connect the output pin '3' of the other gate (SN 7400 has four 2 input NAND gates). Truth table corresponding to the AND gate is given below.

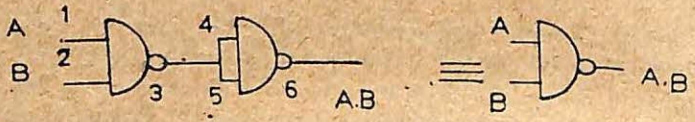


Fig. 54.2

A	B	C
1	1	1
0	1	0
1	0	0
0	0	0

Verify the truth table by feeding the input levels as explained in the previous experiment.

INVERTER

Objective

To study the inverter characteristics.

Experimental Set Up

Equipment needed: as above.
Component required: as above.

Procedure

Connect the circuit as shown in Fig. 54.3. Shunt pins 1 and 2. Feed a signal and observe the output. The state will be inverted. For input of '1', the output is '0' and vice versa.

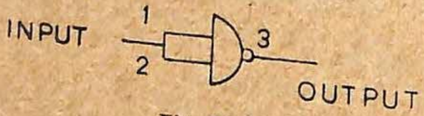


Fig. 54.3

OR GATE

Objective

To construct an 'OR' gate with NAND gates.

Experimental Set Up

Equipment needed: as above.
Component required: as above.

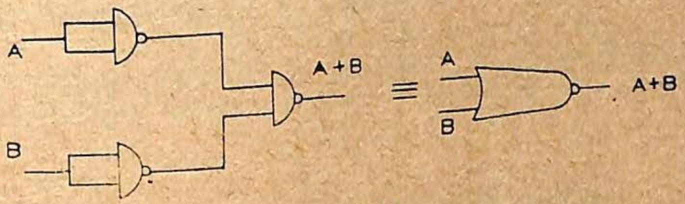


Fig. 54.4

Procedure

From knowledge of Boolean algebra, we know that $\overline{\overline{A}-\overline{B}}=A+B$. Figure 54.4 shows the arrangement of connecting the gates to achieve the above function. Connect the IC pins as shown in the figures. Feed the signals A and B and verify the truth table.

A	B	C
0	0	1
1	0	1
0	1	1
1	1	1

NOR GATE

Objective

To study the functioning of NOR gate using NAND gates.

Experimental Set Up

Equipment needed: as above.
Component required: as above.

Procedure

'NOR' is an inversion of 'OR'. Hence add one inverter to the circuit as shown above. The final circuit is shown in Fig. 54.5.

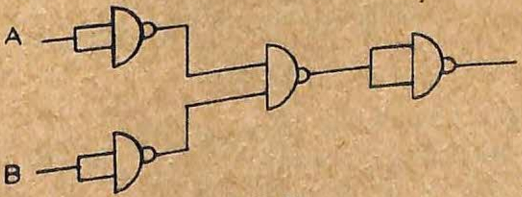


Fig. 54.5

Feed the signals and verify the truth table.

A	B	C
0	0	1
1	0	0
0	1	0
1	1	0

BINARY HALF ADDER USING NAND GATES

Objective

To construct a half adder using NAND gates.

Experimental Set Up

Equipment needed

1. Power supply 5 volts at 100 ma—1 No.
2. CRO or DVM—1 No.

Component required

1. SN 7400 or equivalent chip—2 Nos.

Procedure

Connect the pins of the SN 7400 as shown in Fig. 54.6. For this, plug the IC on to the socket and interconnect the pins of the socket corresponding to the IC as shown in Fig. 54.6.

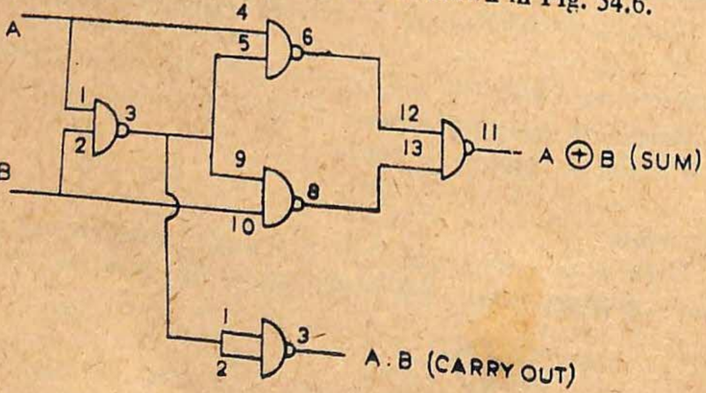


Fig. 54.6

When A is 1 and B is 0, the output at '3' is 1 and that at '6' is 1 and thus pulling the output at '11' to 1. The output from the third pin of the IC number 1 is connected to the invertor made out of the pins 1, 2 and 3 of another IC, SN 7400, which forms the carry genera tor. For the above example when the output at 3 of the first IC is '1' the output of the carry is '0'. When both the inputs are '1' the output at 3 of first IC is '0' and the output at '3' of the second IC is '1' thus generating the carry.

A+B
1+0=1
0+1=1
1+1=10

This experiment verifies the binary half adder using a total of five NAND gates. For generating the '1' and '0' the procedure adopted in the preceding experiments may be followed.

Review Questions

1. What is the nature of output for corresponding to inputs shown in Fig. 54.7 for a NAND gate?

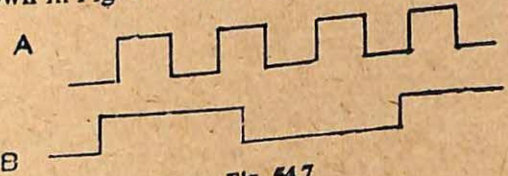


Fig. 54.7

2. What is the propagation delay of an AND gate ?
3. What is meant by fan out ?
4. What is the function of an inverter in digital circuitry ?
5. Draw a half adder circuit using an exclusive 'OR' and inverter.

55

MULTIMETER

A multimeter is a most useful piece of equipment used widely in the laboratory for measuring the basic electrical quantities, voltage, current and resistance. Both DC and AC electrical quantities are often required to be measured. The important characteristics that are required for a multimeter are high sensitivity D'Arsonval galvanometer, low loading effect and good accuracy. Basically a D'Arsonval galvanometer is a DC current meter. For measurements of AC, the AC quantity is rectified and fed to the measuring circuit. A typical multimeter will have a DC sensitivity of 20,000 ohms/volt. There are meters which can have higher sensitivity depending upon the moving coil sensitivity of the D'Arsonval galvanometer used in it.

We may assume the typical sensitivity of a given meter as 0.1 ma FSD. This means that when one volt is applied, the meter takes 1 ma current. Therefore, the meter sensitivity is 1 k.ohm/volt. When a 5V DC input is given to the meter, this will produce a 5 ma current which is 5 times the FSD. This high current will damage the moving coil galvanometer. In order to enable us to measure the 5 volts using the same meter a series resistance of value 4.0 k. ohms has to be added in series with the meter. Similarly for a 50 volts range, a 49.0 k.ohms resistance has to be added in series (refer Fig. 55.1). Like this the DC voltage ranges of the meter can be increased. These resistors are connected through a rotary switch.

Conversion of the meter to measure DC currents of various values is done by using current-shunts. If we want to measure a 10 ma current we have to divert 9 ma current through a shunt

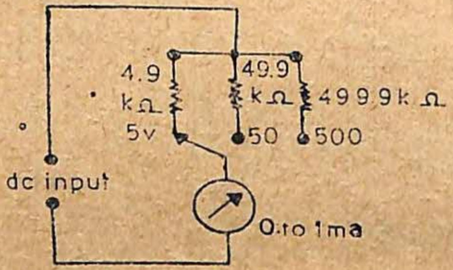


Fig. 55.1

resistance R_{sh} connected across the meter (refer Fig. 55.2). This means that 9 ma current has to be detoured through R_{sh}. The meter resistance is 100 ohms. The current drop through the meter is 0.1 volt. The voltage drop across the shunt resistor should also be equal to this value only. Therefore R_{sh}=0.1v/9 ma=11.11 ohms, has to be connected across the meter. Similarly the values of shunt resistors can be calculated for different current ranges. These shunt resistors connected across the meter which could be selected through an external rotary switch marked in current range.

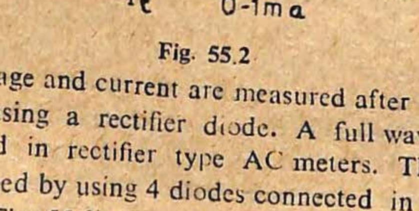


Fig. 55.2

The AC voltage and current are measured after rectifying the AC quantity using a rectifier diode. A full wave rectifier is commonly used in rectifier type AC meters. The full wave rectifier is realised by using 4 diodes connected in the form of a bridge (refer Fig. 55.3), current will always flow through the meter in the direction shown in the Fig. 55.3 for both the positive and negative halves of the input. A resistance R_S is connected in series as shown in Fig. 55.3 to limit the current within the sensitivity limitations of the meter. When the diode is conducting, its forward resistance is very small and so it does not affect the accuracy of the measurement very much. The value of R_S for different ranges can be readily reckoned by interpreting input a-c voltage in terms of the equivalent DC voltage that produces same average output. The full wave rectifier arrangement shown in the Fig. 55.3 if we want to have a full scale range of 0-5V rms, the series resistor required will be the equivalent of 90 per cent of the value required as for similar DC range. (When one volt rms is rectified using a full wave rectifier it produces 1.11 volt DC). For the multimeter under consideration the series resistance is calculated using the formula mentioned below.

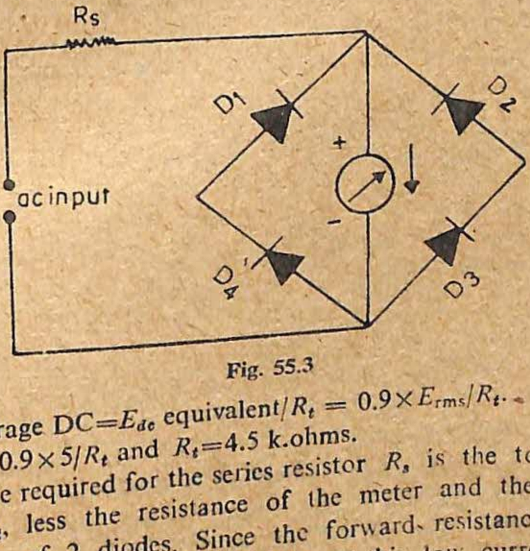


Fig. 55.3

I_m average DC=E_{dc} equivalent/R_t = $0.9\times E_{rms}/R_t$.

1ma=$0.9\times 5/R_t$ and R_t=4.5 k.ohms.

The value required for the series resistor R_s is the total resistance R_t, less the resistance of the meter and the forward resistance of 2 diodes. Since the forward resistance of each diode can be of the order of 1 k.ohm at this low current range of rectification. The series resistance of the meter is 100 ohms, taking all these into consideration, the effective value of R_s= 4.5−2.1=2.4 k.ohms. Similarly the values of R_s for other ranges can also be calculated. What is true for AC current measurements vis-a-vis DC current measurement is also true for AC voltage measurements vis-a-vis DC voltage measurement. The AC sensitivity in this case would be 4.5 k.ohms/volt rms=0.9 k. ohm/volt. By connecting a shunting resistor across the meter, the linearity of the rectifier action is improved. This in turn reduces the sensitivity to 0.6 k. ohm/volt or less. When the same meter is used for AC and DA potentials, a series blocking capacitor is used to isolate the AC measuring circuit from the DC potential. This is done inside the equipment.

The rectifier type meter used for AC measurements has a limitation of frequency. The general range of frequency is 50 to 400 Hz, occasionally it may be extended up to 1 kHz. When it is used to measure any AC potential for frequencies of the order of 20 or 30 kHz, the accuracy comes down very much. The reason for this is not merely the presence of the rectifier. Hence there is no restriction in the use of any type of rectifier in the bridge circuit.

The basic meter movement is used for measuring resistance by combining a voltage source and suitable resistive network as shown in Fig. 55.4. The unknown resistance is connected across

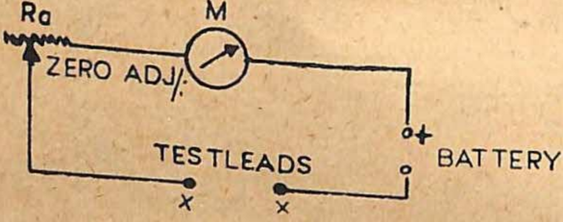


Fig. 55.4

the points X-X and the ohmic resistance is read on the scale calibrated in ohms. This direct reading scale is possible because the current flow is inversely proportional to the total resistance in the circuit for a constant voltage. The potentiometer R_a when adjusted gives necessary corrections for the reduction in the battery voltage. If we use 0-1 ma meter as the basic meter for an input of 1.5 volt battery the total resistance of the circuit is calculated as $R_t = E/I = 1.5\text{V}/1\text{ ma} = 1.5$ k. ohms. The meter resistance is assumed to be 100 ohms. Therefore the variable resistor should be kept at 1.4 k.ohms to produce full scale deflection. (When the test prods are brought together, this 1.4 k. ohms in series with the meter resistance will give rise to full scale deflection which is calibrated as zero ohm). If we connect a known resistance of value, say, 13.5 k. ohms across X-X points, we get a deflection of 1/10th of the full scale. When the value of the resistance to be measured is above this value, the deflection is further reduced and the resolution and accuracy of the measurements decrease. So for higher value of resistance measurement a source voltage of 6 volts or above can be incorporated in the meter circuit using a selector switch.

DC Voltage Measurement

The function switch position is kept in DC volts. Adjust the meter movement trimmer if necessary to make the needle to read exactly zero. This is called the mechanical zero adjustment. Keeping the range at the appropriate (start from the highest range in case of any doubt about the approximate value of the measured variable) level make the measurement. If necessary change the level position to have a large deflection in the meter. When voltages of high amplitude are measured, proper care should be taken to see that the prods are correctly connected and the tips of the same are clean. Measurement of higher voltage in a lower scale is certain to damage the meter movement unless the meter is protected for such exigencies.

AC Voltage Measurement

Keep the function switch position in AC volts. Taking all the precautions mentioned above, make the measurement. Since the frequency limitations of the meter is very low, the meter cannot be accurately be used for measuring higher frequency voltages which may fall even in the audio frequency range.

Current Measurement

Keep the function-switch at the DC/AC current position as the case may be. Taking the precautions about the selection of the range scale, connect the meter in series with the load and make the measurements.

Resistance Measurement

Keep the function switch in ohms and the multiplier in X1 position. Short the prods. Adjust the potentiometer provided in the meter for 'ohms zero adjustment', to read zero in the meter. After this adjustment, remove the short and keep the prods across resistor for measurement. Select the appropriate multiplier factors for measuring different values of resistance. The zero adjustment has to be carried out just before starting the resistance measurement for ensuring accuracy of the reading. The reason being that, the battery gets drained as time passes and the initial voltage is not maintained for a period of time.

56

VACUUM TUBE VOLT METER

Electronic voltmeter using vacuum tubes or transistors is a much improved instrument as compared to an ordinary multimeter, discussed in the previous pages. Because of the amplifying action of the electronic voltmeter, it is capable of providing higher sensitivity and input impedance so that it draws a minimum amount of current from the signal source. In addition, it is able to provide highly sensitive measurements for a wide range of signals. Vacuum tubes and transistors are used to make electronic volt-ohm meter. The vacuum tube being the first to come in the hierarchy of electronic device development, VTVM is older to TVM. Due to the high voltage input nature of the VTVM it commands wider applications in the laboratory. Of late, many devices like FET are developed in the semiconductor technology giving all the salient features like high input impedance and CMR as in the case of a vacuum tube. The later developments in TVM make use of devices like FET for good.

There are different types of VTVM circuits employed. Starting from elementary single tube circuit, we have a wide variety of VTVM circuits employing many desirable features. The Fig. 56.1 shows a two-tube configuration of a VTVM. This circuit is used to measure both DC and AC voltages and resistance. In the circuit shown, the meter movement is connected across the plates of the tubes. The DC potential to be measured is applied to the grid of V_1 through a voltage divider network (refer Fig. 56.2). When there is no voltage applied to the grid of V_1, the potentials at the plates of V_1 and V_2 should be equal and so the meter should read zero. But in practice, the tubes cannot be identical in all

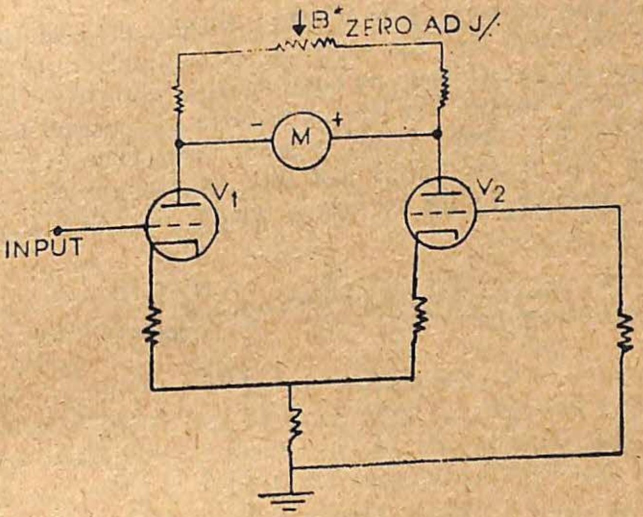


Fig. 56.1

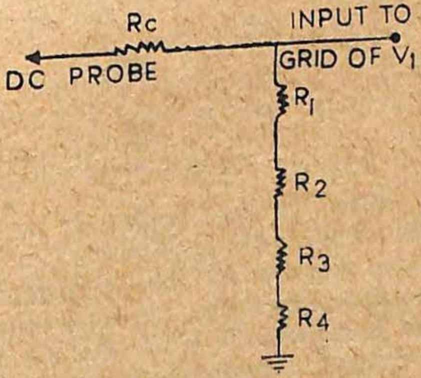


Fig. 56.2

respects and also due to aging, the characteristics vary resulting in an imbalance in the voltages which can be nullified using the zero adjustment potentiometer shown in Fig. 56.1. A positive DC voltage is applied to the grid of V_1 unbalances the circuit by increasing the plate current in V_1 and decreasing that in V_2. The meter movement pointer deflects and this is calibrated in terms of volts. Here, the sensitivity of the measurement is doubled due to the differential connection. Using proper values for the voltage divider, the ranges can be suitably increased.

The input resistance of the VTVM is equal to the sum of the probe resistance and the series resistances used in the range attenuator. The DC input resistance remains constant for all the DC voltage ranges. The input impedance of a general purpose VTVM as AC voltage ranges is much lower than on the DC ranges. This is due to the fact that AC voltages are rectified before applying to the measuring circuit. Fig. 56.3 shows a typical rectifier circuit. The shunting effect of the diode rectifier appreciably reduces the input impedance of the AC voltmeter. Also to be noted that the AC input impedance varies with reference to various ranges. The input to the AC rectifier is coupled through the capacitor to block any d-c voltage in the point of measurement. Therefore it is unnecessary to have a separate AC and output functions because AC position serves both the requirements.

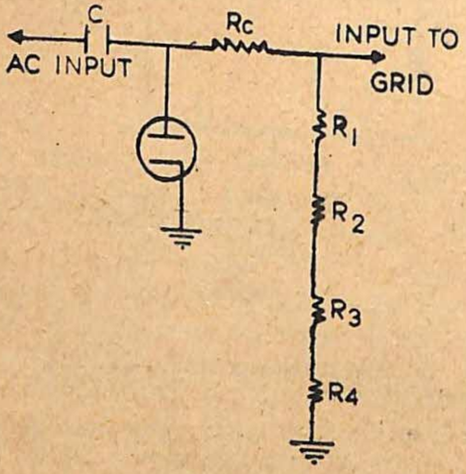


Fig. 56.3

Generally AC scales are calibrated in rms values only. This rms measurements are fairly accurate for sinusoidal voltages whose frequencies fall within the frequency limitations of the meter. This is limited by the frequency response of the instrument. For measurements of nonsinusoidal voltages outside the frequency capabilities of the instrument, the rms scales give only a relative indication of the existence of the voltage. To overcome this handicap many VTVMs are incorporated with a peak to peak function and special peak to peak scales for the measurement of nonsinusoidal waveforms.

RF probes are widely used in VTVMs to extend the frequency range of the instrument. A solid state or vacuum tube diode in the probe rectifies the RF signal. The design of the probe and the components used ensure a useful measurement well beyond the AC frequency limitation of the instrument. When RF probe is used, function switch is put in the DC range. The rectified RF voltage then directly goes to the DC input of the instrument. These readings are relative rather than absolute measurement of RF voltage.

The DC voltage range is extended using high voltage DC probes. This probe contains a specially manufactured multiplier resistor which extends the DC voltage ranges. For example, a probe with a factor of 100 as multiplier extends a 50 volt DC to 5000 volt DC. The value of the probe resistor say, R_p required to multiply the range of the meter by a factor S is calculated from the following equations.

$$R_p = R_e + (S-1)\, R_{in}$$

where R_p is resistance in ohms of high voltage multiplier.

R_e is resistance in ohms of isolating resistor in the DC probe.

R_{in} is input resistance of the VTVM.

For a value of $S=100$, $R_e=1$ meg ohm and $R_{in}=10$ meg ohm, $R_p=991$ meg ohms.

The decibel measurement is also possible in VTVMs. The decibel measurement is a logarithmic unit.

decibel, $dB=10 \log_{10} \dfrac{P_2}{P_1}=10 \log \dfrac{E_2^2/R_2}{E_1^2/R_1}$ where P_2/P_1 is the ratio of audio power levels being compared, E_2, E_1 are audio voltages appearing across the respective loads R_2, R_1.

When $R_2=R_1$, $dB=20 \log E_2/E_1$.

When $R_2 \neq R_1$, $dB=20 \log E_2/E_1+10 \log R_1/R_2$.

The decibel scale is generally imbedded on the VTVM's DC and AC scales.

The measurement of resistance in the VTVM is accomplished by placing an unknown resistance in series with an internal voltage source and now divider network used for ohms range only. The voltage drop across the unknown resistor is then applied to the grid of the tube which measures the DC voltage drop. The simplified circuit shown in the Fig. 56.4. When the

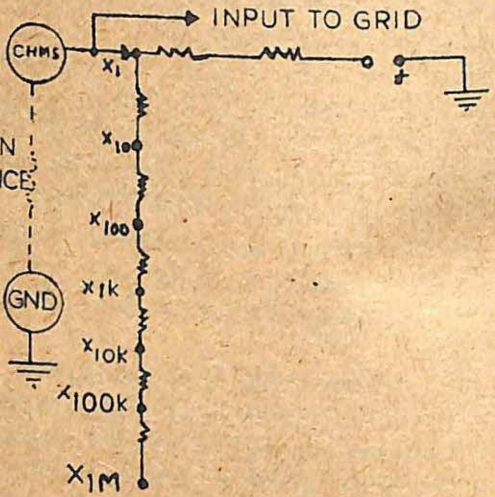


Fig. 56.4

unknown resistor is connected between the ohms and ground terminals a current from the voltage source flows through this resistor which is connected in series with R_{01} and R_{02} and that portion of the resistance divider selected by the position of the range switch. The voltage drop across the unknown resistor caused by the current flow from the voltage source supplied to the tube which causes a meter deflection. This deflection is calibrated in terms of resistance.

DC current measurement is made by flowing the current across a suitable resistor and measuring the voltage drop across it. This voltage is calibrated in terms of current. For different ranges, suitable resistors are chosen. For AC measurement the drops is rectified and the rectified voltage is measured. The accuracy of this measurement is the same as that of AC voltage measurements explained previously. Generally the overall accuracy of this type of instrument is ±3 per cent.

Applications

Switch on the equipment. Allow a period of about 30 minutes for warm up to stabilise the circuit. If there is a calibration provision available in the meter, put the switch to the calibration position and watch for full scale deflection. If the deflection is not coming to read full scale, adjust the calibration potentiometer to read full scale. Switch back to the highest sensitivity position and with input shorted adjust for zero reading if necessary, by the zero adjustment potentiometer. Now the equipment is ready for use. A positive DC voltage is to be measured, short the negative and the ground points in the input terminals and feed the signal across the positive terminal and the ground with the sensitivity position at the lowest (at the highest range for DC). Then, if necessary, lower the range position of the switch to get maximum deflection without exceeding the full scale. For negative voltage measurement, short the positive and ground terminals and feed the input signal between the negative and ground terminals and repeat all the procedures mentioned above.

Put the function switch in the AC voltage position. For ac voltage measurements, use the AC probe provided for this purpose. Don't forget to ground the clip provided in the AC probe. Keep the tip of the probe at the point where voltage is to be measured. Observing the range precautions mentioned earlier, make the measurements.

Keep the function switch in the ohms position to measure resistance. Selecting a proper range, connect the resistor across the DC terminals. Note the deflection in the meter, observing all the range precautions mentioned earlier.

57

TRANSISTOR VOLTMETER

The development of semiconductor devices has given a boost to the technology of instrumentation. The availability of dependable transistors has improved the sensitivity factor of any equipment development. TVM is an improved version of VTVM using semiconductor devices. This type of voltmeter is operated with battery, at once freeze the equipment from the AC hum pick-up and at the same time provides high amplification. Transistor voltmeter unlike its predecessor VTVM does not require any heater current and saves power on that count. This battery operated equipment is very handy even for field applications. With all the advantages of compactness and greater reliability of a solid state instrument, there are some disadvantages too. Circuit arrangements using conventional bipolar transistors have tended to be more and more complex in overcoming the two built-in limitations of transistor, viz., low input impedance and temperature dependence. However, the later developments in semiconductor technology has given rise to unipolar transistors like FET and MOSFET. These devices have improved the reliability and temperature problems which the bipolar transistors bothered the circuit designers.

For all practical purposes a TVM is a VTVM only. All the measurements which can be done with a VTVM can be done with a TVM also. The FET input amplifier used in the TVM gives very good input impedance, sometimes higher than that of a vacuum tube. The basic circuit used is shown in Fig. 57.1. The input voltage is fed to the FET input amplifier after attenuation. The differential amplifier senses this change in the bias

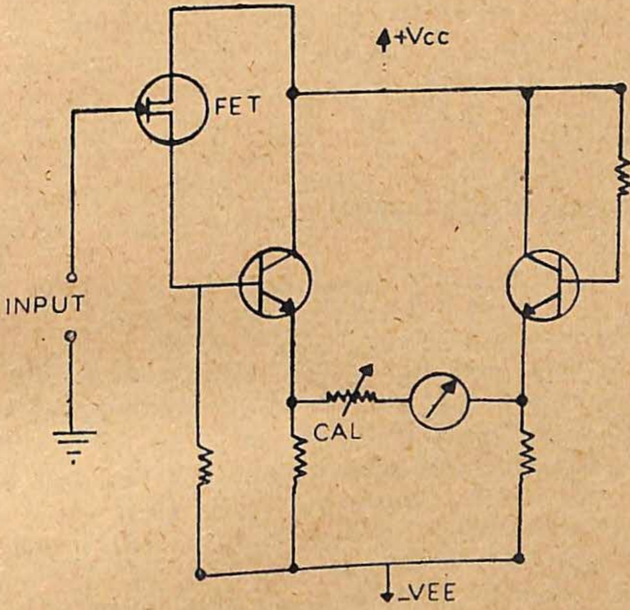


Fig. 57.1

condition and provides the appropriate changes at the emitter points. That is sensed by the meter which is calibrated in terms of voltage. The calibration potentiometer provided in the circuit enable the user to adjust the meter position. A suitable attenuator circuit caters to the needs of different levels of input voltage. At higher voltages, proper insulation precautions are taken.

58

TRANSISTOR TESTER

The failures very often noticed in transistors are due to: (i) shorting of any two junctions, (ii) open circuiting between any two junctions, and (iii) leakage and so on. A quick check to determine whether the given transistor is good or bad, an ohm meter check can be resorted to. The ohm meter has a voltage source which is already built-in. There is a series limiting resistance which protects the transistor under test. The following circuit shown in Fig. 58.1 gives as a quick method of checking the transistor connected in the common emitter configuration. By means of the switch, reading on the meter is first obtained

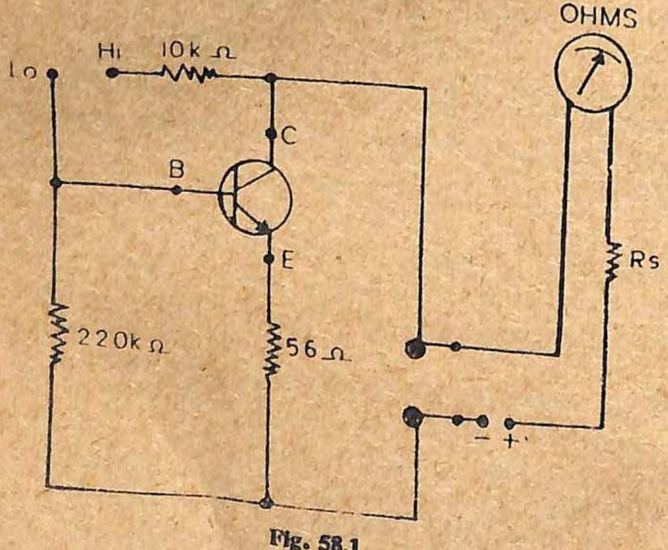


Fig. 58.1

under the condition of zero bias on the base which is returned to the ground through a 220 kilo ohms resistance. This collector current reading is called the *Lo* reading. When the switch is put in the *Hi* position, the base is biased by allowing the base current to flow through the 10 kilo ohms resistor and the new value of the collector current called the *Hi* reading is obtained. The net change in the current between the *Hi* and *Lo* readings then gives the comparative DC current amplification factor.

Transistor testers and analysers are far more reliable instruments for testing transistor parameters. A transistor tester should be able to provide direct reading values for (i) forward gain in the common emitter configuration which is denoted as h_{fe} for AC gain and h_{FE} for DC gain and (ii) the collector to base leakage current I_{CBO}. The second measurement is generally regarded as the most significant one in the aging process of a transistor. It is comparatively difficult to measure because of the extreme temperature sensitiveness of this parameter. This parameter is pretty high in a germanium device as compared to a silicon device. These two tests are the basis for most of the commercial type testers. More expensive tests of transistor parameter are carried out in a laboratory type transistor testers called curve tracers.

The proliferation of transistor development has given rise to the introduction of different kinds bipolar, unipolar and MOS devices. The measurement of all parameters of such devices have been a very difficult task and continuous development are being carried out to bring out suitable test equipment for the measurements.

The incircuit semiconductor testers are also available in the market. One such model is marketed by M/s. AEL Model No. 259. This equipment measures the parameters of diodes, transistors and FETs, both incircuit and out of circuit.

A curve tracer is, by and large, an ideal equipment for observing the various transistor characteristic curves displayed on a CRT. The curve tracer type No. 576 marketed by M/s. TEKTRONICS is a very handy equipment. Various controls and adapters for measuring a wide range of transistors including FETs, SCRs, UJTs, etc., are available. Steps of current of voltage in staircase form is selected by the corresponding control and applied to the transistor under test which produce a family of curves. From the common-emitter configuration, *B* of the transistor can be easily read out. The voltage can be varied and the transistor characteristics can be studied under near full ratings.

59

UNIVERSAL IMPEDANCE BRIDGE

Measurement of resistance, capacitance and inductance is a very often required activity in an electronics laboratory. Universal impedance bridge is a versatile equipment to carry out all the above measurements. There are many makes of universal impedance bridge in the market which can measure resistance, capacitance and inductance with high accuracy over a wide range. Resistance measurement is done using a Wheatstone's bridge. Inductance and capacitance are generally measured by comparison with a standard capacitor in R-C ratio arm circuits.

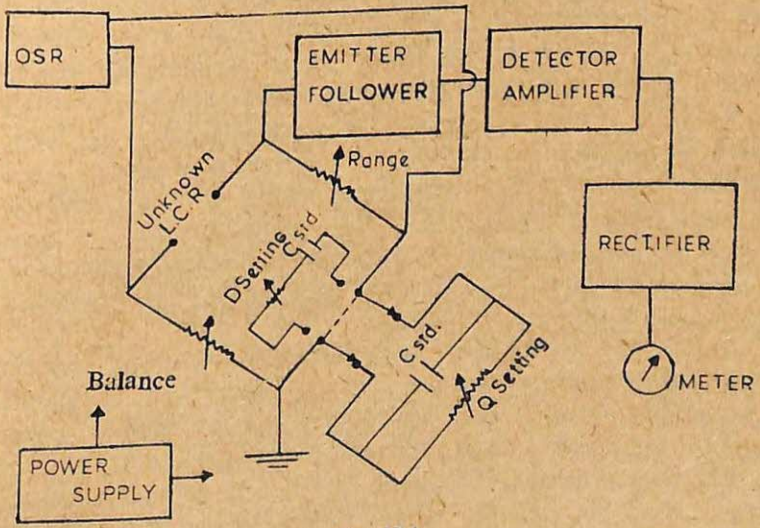


Fig. 59.1

A block diagram of a universal impedance bridge is given in Fig. 59.1. An internal oscillator of, say, 1 kHz frequency is used for exciting the bridge for AC measurements. Provision is generally given to excite the bridge with an external oscillator also. The oscillator excites the bridge. The output from the bridge is fed to the detector amplifier through an emitter follower circuit. The amplifier output is rectified using shunt diode and then fed to the meter. This enables the meter to move always to one direction for all AC measurements. Circuit nuances are provided to protect the meter from higher voltages by connecting limiter diodes. For DA resistance measurement separate provision is available to excite the bridge with DC voltage.

To improve the range of measurement multipliers are provided. High precision metal film resistors of good temperature stability are used in the multiplier stage. The multiplier ranges are provided in decade steps. Any variation in the value of the multiplier resistor either due to aging or temperature will affect the accuracy of measurements.

To measure resistance the following steps have to be gone through. Switch on the equipment. Allow for a warm up period of 15 minutes. Choose the excitation for DC or AC measurements, as required. Connect the resistor across the terminal provided in the equipment. If the approximate value of the resistor is known then choose the suitable multiplier range. If the value is not known start from the highest range. Keeping the sensitivity control to mid range, adjust the balance control for a null deflection. If necessary reduce the range or increase the range depending upon whether the meter movement is small or very fast. Get a null for the particular setting of the sensitivity control. Then increase the sensitivity control position and again adjust the balance control for null. Do this for the highest setting of the sensitivity control. Read off the value from the multiplier and the fine control settings.

To measure capacitance, keep the excitation switch in AC measurement and the function switch to capacitance. Taking the precautions for the range selection adjust the balance control and the loss factor control simultaneously to get a null.

The same procedure is followed for inductance measurements also. Here the function switch should be put into inductor position.

60

SIGNAL GENERATOR

A signal generator basically consists of an oscillator, a power amplifier and a buffer amplifier. The buffer amplifier is provided between the oscillator and the power amplifier to give isolation and to prevent variation of oscillator frequency due to load fluctuations. The block diagram of a typical signal generator is shown in Fig. 60.1. The signal generator will usually have provision for both internal and external modulations.

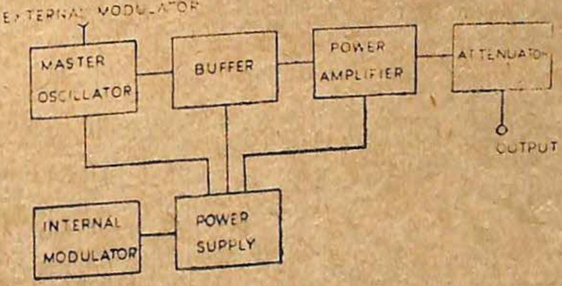


Fig. 60.1

A master oscillator will be either an RC type oscillator or an LC type oscillator for lower or higher frequency ranges. The tuning element in the oscillator is generally a variable capacitance. In microwave frequency ranges a klystron with variable cavity is used as an oscillator.

In the RF frequency ranges shielding plays a very important role in preserving the stability of the oscillator and to reduce stray coupling etc. The frequency variation in the oscillator which is caused due to load variations can be reduced using a buffer amplifier and using a regulated power supply in the circuit.

Another source of frequency instability is temperature changes. The ambient temperature of the environment should be kept reasonably constant for good performance of the equipment. Some time should be given to normalise the various parameters before using the equipment. Otherwise there could be fluctuations in the output at the signal source.

Another important block in the instrument is the attenuator. A typical one is as shown in Fig. 60.2. A good attenuator is a very important link in the signal generator. There are different kinds of frequency compensated attenuators. Each step in the attenuator is carefully shielded to give a high degree of isolation of the output from the input of the attenuator. The output impedance of the attenuator should be made equal to the load impedance for maximising the power transfer efficiency. When the impedance and output impedance are different, the mismatch can be avoided using a matching pad.

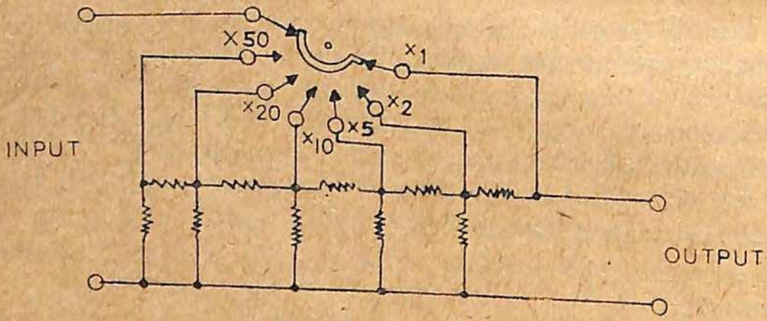


Fig. 60.2

A matching pad is a two way mask that makes the load impedance look like the generator impedance, and vice versa. Modulation signals are provided through an internal oscillator source. A provision is generally made for carrying the modulation level. The internal modulation frequency is generally a fixed one, say, 400 or 1000 Hz. Most signal generators have provisions for external modulation. FM and AM provisions are given in many signal generators. The percentage modulation of the AM and frequency variations of the FM can be read off from the meter provided for this purpose. Many RF signal generators are provided with internal crystal oscillator which provides frequency check signals of 1 kHz apart over the band.

61

CATHODE RAY OSCILLOSCOPE

Cathode ray oscilloscope is a highly versatile instrument which adorns an electronics laboratory. When properly used a CRO is capable of measuring all electrical quantities and functions. A CRO is mostly used for displaying waveforms. Comparison of phases of two signals can be done by using a double beam CRO. Some stray or transient phenomenon could be recorded in a storage oscilloscope for detailed analysis at a later period. Delay line provisions available in certain type of oscilloscopes enable the circuit designer to study the behaviour of the waveform after deliberately introduced delay time. The triggering facilities available in CROs enable one to trigger the given waveform at any desired point of the waveform for detailed analysis. The high sensitivity nature of the amplifier circuit used in the CRO can be gainfully used in finding stray pick-up, narrow spikes and other transient phenomenon in a given circuit. These informations are very vital to the circuit designer to perfect the system. Thus a CRO is an unmatched companion, guide and philosopher to the circuit designer.

The mainstay of a CRO is a CRT. The electron deflection in the CRT will go on to investigate the fundamental types of waveform patterns obtainable with an oscilloscope. The patterns formed on the CRO screen result basically from the effect produced when a narrow beam of electrons is shot from the 'electron gun' assembly and impinges on the phosphorescent coating of the tube. The spot of light focussed on the screen due to the emission of electron is deflected horizontally and vertically by applying voltages to the respective plates that makes possible the waveform patterns on the screen. The arrangement of the electron gun assembly for electrostatic deflection is shown in Fig. 61.1. The electron gun consists of a heater with its directly heated

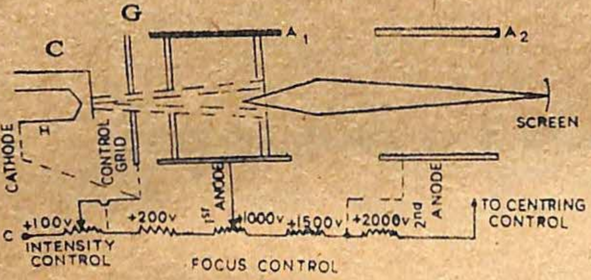


Fig. 61.1

cathode, the control grid, the 1st and 2nd anodes. The control grid is cylindrical in shape with small aperture in line with the cathode. The electrons emerge out of the aperture as a slightly divergent beam. The quantity of electrons making up the beam is controlled by negative bias supplied by the grid. The intensity of the phosphorescent spot depends upon the beam current which in turn depends upon the quantity of electrons emitted from the cathode and so the knob controlling the grid bias is called the intensity control.

The diverging beam of electrons are brought to a focus on the screen using two anodes which are positively biased. These two anodes focus the electrons as a lens focusses a beam of light as a spot. These anodes work as electronic lenses. In line with the opening in the grid cylinder is a corresponding opening in the narrow cylinder that constitutes the first anode and is highly positive with respect to the cathode. A wider cylinder following the 1st anode with its aperture in line with the electron beam is operated at a still higher positive potential. The 2nd anode is called the accelerating anode. The control by which the electron lens is caused to focus the electron beam exactly on the screen surface is the potentiometer providing variable voltage to the 1st anode is called the focus control. When this control is turned to either side of the correct focussing position the spot becomes larger and looks blurred. When the spot is properly focussed it will produce a narrow sharp trace on the CRT screen.

There are 2 sets of deflecting plates called vertical deflection and horizontal deflection plates. With no potential applied to the deflecting plates the beam passes through both the sets of plates and appears as a bright spot at the centre of the screen. If a positive potential is applied on the top one of the vertical plates, the beam will move upward by an amount depending upon the potential applied. This is because the stream of electrons are attracted by electrostatic field applied to the plate. If a negative voltage is applied to the same top plate, the beam will move downward due to electron repulsion. The procedure, in a general purpose CRO is to ground one of each of the pairs of deflecting plates so that the deflection voltages are applied to only one plate in each pair. An AC voltage is applied to the vertical deflection plate causes the spot to move up and down alternately. When a 50 Hz AC signal is applied, it causes 50 up and down movements in a second but the visual indication will be a straight line. This is due to what is called the phenomenon of the persistence of vision characteristics of the human eye. The flicker will be noticeable at frequency less than 20 Hz.

Horizontal deflection is produced in precisely the same way on application of a voltage between one of the horizontal plates and ground (refer Fig. 61.2). When a voltage is applied to the horizontal plate it produces a horizontal base, sometimes called the X-axis and is made to represent time. The vertical or Y-axis deflection represents the applied signal voltage and its peak to peak amplitude will thus represent the maximum positive and negative swings of the applied signal. Since the result produced by the application of any deflection voltage is instantaneous

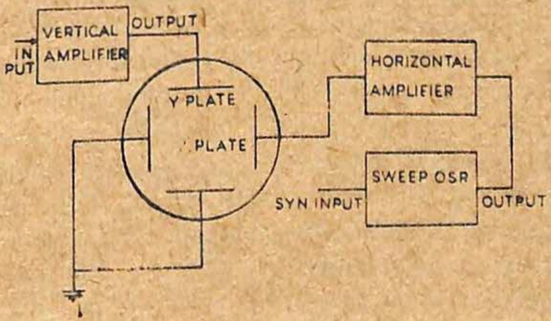


Fig. 61.2

response, we have in the CRT, the possibility of a visual indication.

CRO can be represented by a block schematic diagram as shown in Fig. 61.3. The block consists of a vertical attenuator to attenuate the input voltage suitable to feed the vertical amplifier. The output of the vertical amplifier taken from a differential combination is fed to the vertical plates of the CRT. A portion of the input is used to synchronise the sweep generator output which is fed in turn to the horizontal amplifier. The horizontal amplifier output is fed to the horizontal deflection plates of the CRT. There are two power supply system namely (i) low voltage supply and (ii) high voltage supply. The low voltage supply consisting of a few voltages which are less than 300 volts provides power to all the amplifier systems. The high voltage supply provides power to the various points in the CRT as shown in Fig. 61.1.

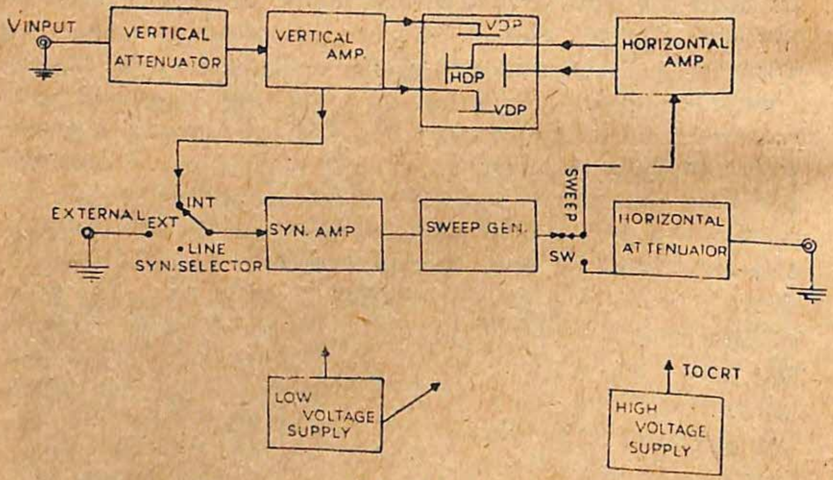


Fig. 61.3

Vertical Attenuator

An oscilloscope has to respond different voltages for display. The voltages may be a few millivolts or a few hundreds of volts. This wide span of voltage levels are to be accommodated in the circuit. This is best done using input attenuator. An input attenuator feeds a constant voltage for all ranges to the input of the Y amplifier. A carefully designed frequency compensated attenuator network is a prerequisite of any good oscilloscope design. Since the range of frequency of the input is fairly wide for the oscilloscope, utmost care should be taken in the selection of components or else there will be drastic change in the input impedance. A balanced vertical attenuator circuit is shown in Fig. 61.4.

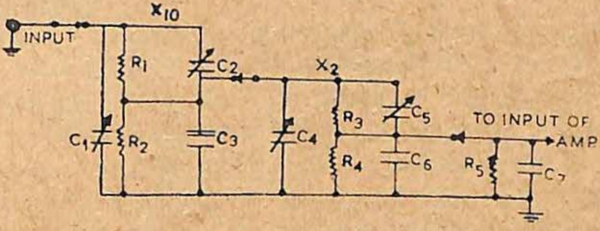


Fig. 61.4

Vertical Amplifier

The vertical amplifier determines the sensitivity and frequency response characteristics of the oscilloscope. The gain-bandwidth product is a constant factor for a given amplifier. The sensitivity of the amplifier can be improved only at the cost of frequency response and vice versa. So, the sensitivity of the oscilloscope is always specified as so many mv or volts required per cm of vertical deflection at midband frequency and up to, say, $-3dB$ point. For example if an oscilloscope specifies 10mv rms as its sensitivity cm of vertical deflection, for a frequency of say, 1 MHz it means that the amplifier may response to this extreme frequency of 1 MHz with an amplitude of 7 mv instead of the midband value 10 mv rms. A typical amplifier circuit is shown in Fig. 61.5. The input impedance of the vertical amplifier is generally mentioned as, say, 1 meg ohm shunted by around 70 pF for shielded cable input. The input impedance specification is dependent on the frequency. For example at very high frequencies of the order of 500 MHz, input impedance is shown as 50 ohms.

Synchronisation Amplifier

To view the waveform in the oscilloscope without any jittering effect, a portion of the input voltage is taken, amplified

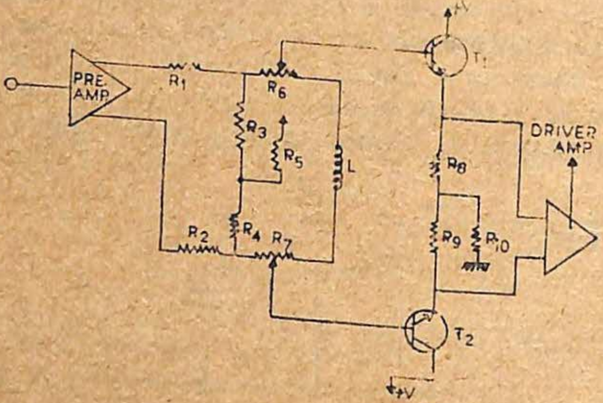


Fig. 61.5

and injected into the sweep generator to lock the sweep generator output to the input frequency. This gives a good waveform stability.

Sweep Generator

Sweep oscillator generates a sweep frequency which is used as time base to control the *X*-axis of the waveform. It is synchronised to the input voltage as explained above or synchronised with an external input of our choice.

Horizontal Amplifier

Horizontal amplifier serves two purposes, viz., (i) in ordinary waveform presentation, it amplifies the time base voltage from the sweep oscillator providing a control for the width of the

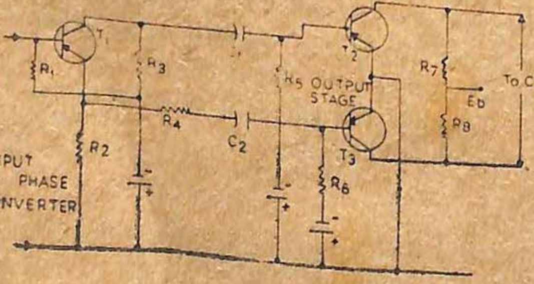


Fig. 61.6

resulting pattern and (ii) when switched out off the sweep position it accept a signal applied to the *X*-input point and amplifies it to the desired amount to provide a necessary amount of voltage to the horizontal deflection plates. A typical circuit of a horizontal amplifier is given in Fig. 61.6.

Power Supply

The positive low voltage supply which varies upto 300 volts provides necessary power to the various circuits shown in the block diagram (refer Fig. 61.3). Some of the voltages which provide power to sensitive circuits are regulated. The ripple content is kept to a low value to ensure waveform clarity. Noise is also kept to a minimum through proper shielding. The high voltages required for the CRT are generated by a doubler action of diodes and capacitors, (refer Fig. 61.7). High voltage supply provides a few ma currents only.

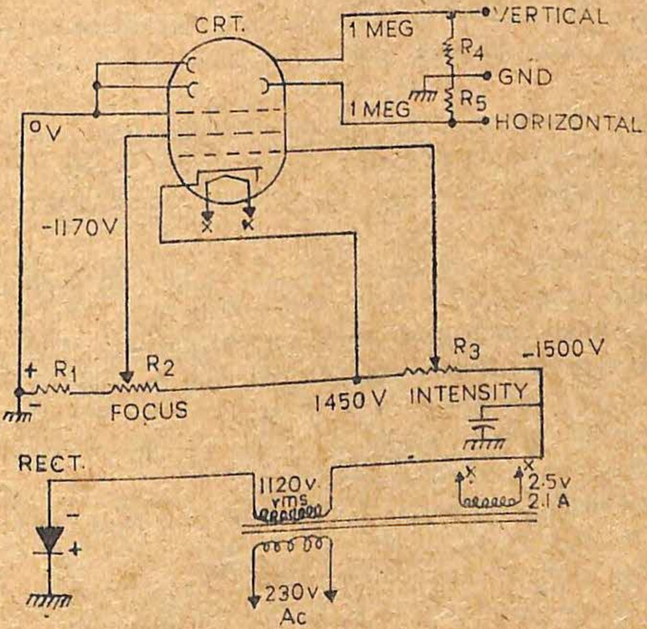


Fig. 61.7

Applications

Familiarisation of various controls.

Focus: This control is adjusted in conjunction with the controls marked as intensity and astigmatism in order to get the sharpest trace on the screen. The intensity control is adjusted for desired brightness of the trace. Excessive brightness will burn the phosphorescent screen of the CRT. The astigmatism control is used in conjunction with the above two controls for the sharpest trace.

Vertical range or multiplier: This is a calibrated step attenuator which selects the constants of a voltage divider in the vertical input circuit.

Vertical gain control: This is a potentiometer which is continuously variable over any selected range of the vertical amplifier. When this control is put in the cal position, the reading shown corresponds to the exact multiples of the range selected in the vertical amplifier.

Horizontal gain control: This is a potentiometer which provides a continuous control of the amplitude of the signal fed to the horizontal amplifier.

Horizontal and vertical centring: This potentiometric control provides the left or right and up or down positioning of the trace.

Coarse frequency control: A rotary switch selects depending upon its position the frequency range of the sweep oscillator. This is marked in terms of sec, millisec and microsec in the front panel.

Fine frequency control: This is a potentiometer which operates in conjunction with coarse frequency selector which enables to select any sweep speed between any two steps of the coarse control. When this potentiometer is kept in the cal position, the frequency displayed on the CRT for any input given to the vertical amplifier is exactly as marked against the coarse setting of the sweep selector.

Synchronisation selector: This is a special type of switch which enables one to select any mode of synchronisation like internal, external or line synchronisation. When the switch is put in the external and fed an external signal, the oscillator gets synchronised with the external input. When it is put in the 'line' the sweep is synchronised to the line frequency.

Synchronisation amplitude: This is a potentiometer which varies the level of synchronisation signal which is coupled to the sweep oscillator. This control is set at the lowest level at which it will lock the signal.

Trigger +ve and −ve: This selects the triggering of the waveform at its positive going or negative going half of the input depending upon its position.

Determination of phase relationships: An oscilloscope can be used to find out the approximate phase relation between two signals fed to the horizontal and vertical amplifier circuits of the CRO through certain resulting patterns known as Lissajous Figures. The test set up is as shown in the Fig. 61.8. The sweep position is put in the external position in the CRO.

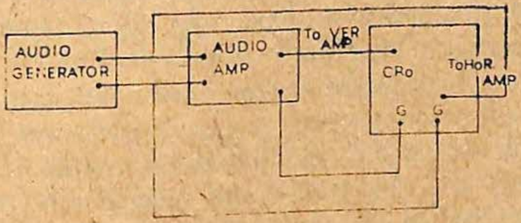


Fig. 61.8

Oscilloscope probes: A probe is an important part of the CRO for measurements. There are many reasons why an ordinary pair of wires cannot be used for the purpose of measurements. The stray capacitance which is produced between the wire and any metal object can work havoc in measuring high frequencies. The stray capacitance varies with the length of the wire and reduces the input impedances also at higher frequencies. Another problem is the so-called antenna effect. That is unshielded scope lead would act as an antenna and picks up any electromagnetic interference from a radio station or a TV broadcasting stations which are close by. For these reasons the probe is connected to the vertical input through a coaxial cable. The coaxial cable does not pick up EMI signals. Because of the definiteness of the capacitance which is so much per foot or metre, a suitable length can be chosen to bypass in frequencies above a required range. A probe circuit designed to minimise the effect of the capacitance is shown in Fig. 61.9.

The coaxial picks up a voltage from the voltage divider $R_1 - R_2$. The resistances can be chosen to provide a suitable attenuation

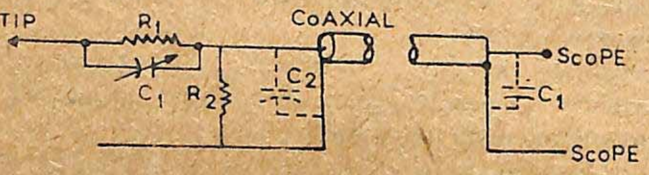


Fig. 61.9

ratio, say, 1 or 10. The probe is marked '10X Atten', then it means that the scope display is to be multiplied by 10 for absolute measurement. The variable capacitance C_1 is used to minimise the effect of capacitance C_2 and C_3 which are produced by the coaxial cable and the scope input. The C_2 and C_3 capacitances being parallel to the input, they try to bypass the high frequency signals to the ground. This will cause the roundness of the corners on displayed square waves. The variable capacitance C_1 added in the circuit comes in series with the parallel combination of C_2 and C_3 resulting in the overall reduction in the value of the capacitance. This reduction in the effective capacitance reduces the signal leakage to the ground. Since C_1 is provided as a trimmer capacitance, its value can be adjusted by the scope operator until the scope displays a square waveform with good fidelity.

Demod probe: A demodulator probe is used to examine modulation waveforms. The upper frequency limit of an ordinary probe is only a few 100 kHz. The RF waveforms of a radio which is a few tens of MHz can be observed by using a demod probe. Circuit shown in Fig. 61.10 is a typical half wave type demod probe. Basically the circuit is a broad band crystal detector with RF filtering on the output. Common commercial demod probes may easily extract the signal from a carrier upto 200 MHz.

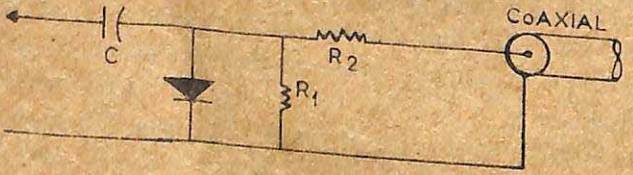


Fig. 61.10

Special purpose probes: There are many kinds of probes for any conceivable applications. The probe in Fig. 61.11 is an example of frequency sensitive probe. There are high voltage probes used to measure very high voltages of the order of few tens of kilo volts on a CRT directly. There are special types of current probes to measure alternating or direct current in a circuit without opening the circuit. Besides the passive probes, there are many kinds of active probes which use built-in amplifiers. These minimise the effects of EMI pick up and reduces the loading effect on the circuit under test.

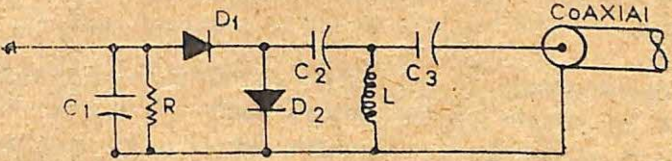


Fig. 61.11

62

DIGITAL FREQUENCY COUNTER

The developments in the digital circuit technology and the invention of simple display systems such as nixies, alpha numerical tubes, LEDs, etc., has advanced the scope and range of various kinds of electronic equipment in the measurement of parameters like frequency from a few Hz to gega Hz and improving the accuracy of voltage measurements to microvolts level. Frequency counter is an important piece of equipment in any modern electronic laboratory. There are occasions in which a measurement of frequency from a signal of amplitude as low as a few millivolts has to be carried out. Some of the modern counters have such a high sensitivity as to enable it to measure the frequency of the signal accurately even when the signal strength is as low as 10 mv or less. The advent of microcomponents has advanced the range of the frequency counter.

Before discussing the details of digital counting instruments, it is well to recall the elements on which the electronic switching processes are based. Extensive use of decade counters and the digital logic elements—the NOR gate, the NAND gate and the inverter with high speed capabilities play a vital role in the process of digital counting. A few logical elements used in the circuit are as given below.

RTL = Resistor Transistor Logic
DTL = Diode Transistor Logic
ECL = Emitter Coupled Logic
TTL = Transistor Transistor Logic

Each of the above forms of gate design has particular advantages. The RTL and DTL forms are economical types. The ECL form features higher switching speeds. While TTL represents a widely used type combines the advantages for its flexibility, for its compatibility with DTL and other types. In addition to the basic logic elements, there are other components, which are of equal importance, like comparators, clocks, adders, shift resistors and memory elements. Many of the logic elements are the products of the technological revolution in the digital electronics known as the median scale integration (MSI). This technology combines as many as ten functions in a small compact chip.

The process of counting the frequency is basically a process of counting pulses. The input waveform is shaped and sharp pulses are generated using a Schmitt trigger, differenciator and rectifier circuits. Figure 62.1 explains the various process involved in

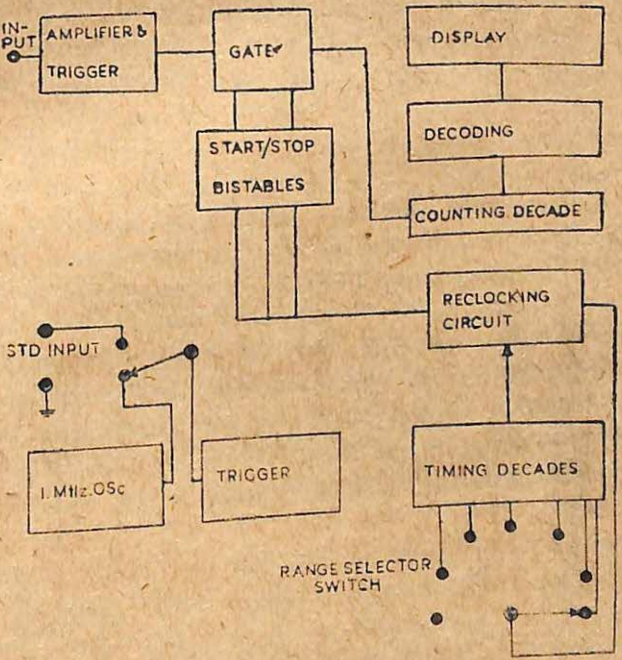


Fig. 62.1

the counting. The amplifier and trigger block consist of an amplifier circuit and a Schmitt trigger circuit with associated shaping circuitry. The amplifier is generally a high input impedance device. The amplifier gain and frequency response play an important role in determining the sensitivity and the frequency limitations of the counter. The amplified signal is used to trigger a Schmitt circuit to generate good square wave output. Schmitt trigger's capability also determines the frequency limitation of the counter. The square wave output is differentiated and positive pulses are segregated. Then they are fed to the counting circuit through a gate.

Internal oscillator acts as a source of generating gate signals. The oscillator chosen is generally a crystal type with oven control facility to improve upon its stability. The output of the oscillator fed through a trigger source and then to timing the gates which consist of decade counters available as integrated chips. A selection range is provided externally to select different gate timings to suit the measurement constraints. The output of the timing decades is sent through the reclocking circuit to enable a start stop bistable which in turn opens and closes the gate for the incoming signals from the amplifier-trigger circuit.

The gate allows a number of pulses for the duration for which the gate is made open through the external time base selector switch. For example, the time base selector switch is in one second position, then the gate is kept open for a period of one second and the pulses allowed to pass through are also counted directly as frequency up to a resolution of one Hz. If the switch position is in 0.1 sec., say, then the pulses allowed to pass through is naturally ten times less than that for the previous case. The output display, therefore, has to be read as decade multiple. Depending upon the positioning of the switch, the display annunciator displays kHz for one millisecond position of the switch.

The pulses coming out of the gate go through a series of counting decades whose output which is in BCD is fed through decoding circuit. The output of the decoding circuit lights up the respective figures of the display device which may be nixie or LED.

Many frequency counters can also be used as a unit for measuring period of any input signal. Many modifications are possible to convert a basic frequency counter into a time interval measurement unit, frequency ratio measuring unit, etc.

Provisions are also made to drive the counter with external gating signal. A self check is provided in the counter to see whether the counter is working or not without giving an external signal. For this the output of the internal oscillator is fed to the input through a switch. When the switch is put in the self check mode this signal from the internal oscillator goes through the amplifier stage and other circuits to display the frequency.

63

DIGITAL VOLTMETER

Voltage measurement is very often required to be done in any electronic circuit assembly. The accuracy and the resolution of the measurement vary from requirement to requirement. In high precision works the accuracy and resolution of measurement play a very important role. A digital voltmeter is a very suitable equipment for accurate and high resolution measurements. The measured quantity is displayed as digits and so the error in reading out the value, unlike in the analog meters, is not there. High input impedance is also possible in a digital voltmeter. This will go a long way in meeting the stringent measurement requirements of some of the critical circuits.

The state of art in the design of digital voltmeter has undergone many desirable changes in the recent past, thanks to the development of electronic devices. The most important aspect in the digital voltmeter design is that requiring the conversion of analog signal into a digital one which is generally called A-D conversion. There are three main principles as listed below.

1. Comparison principle, using successive approximation method.
2. Counting principle using a voltage to frequency method.
3. Integrating principle, using a ramp to accomplish a voltage to time method

There is a fourth method called 'dual slope' method which is a modification of the third method mentioned above. This method has an advantage in that it can cancel the noise and lessen the possible errors in the voltage to time measurement.

In this article the principle of double integration method only is dealt with.

Dual-slope integration technique is simple and has the desirable characteristics of stability and accuracy. A block diagram of this is shown in Fig. 63.1 (a). The figure shown in 63.1 (b) reveals the charging and discharging slopes of the signal. The block diagram of Fig. 63.1 (a) is the one dealing with a dual slope A-D converter consisting of five basic blocks. The

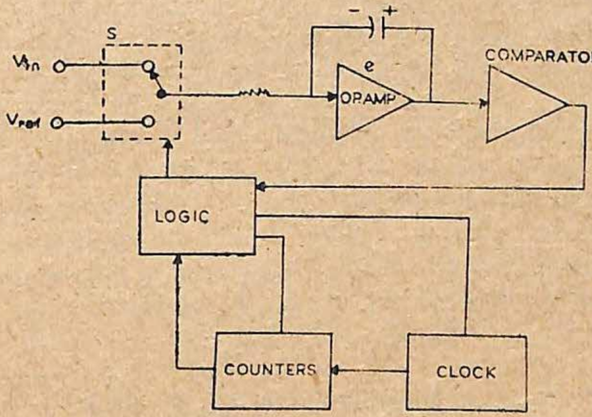


FIG. 63.1(a)

Fig. 63.1 (a)

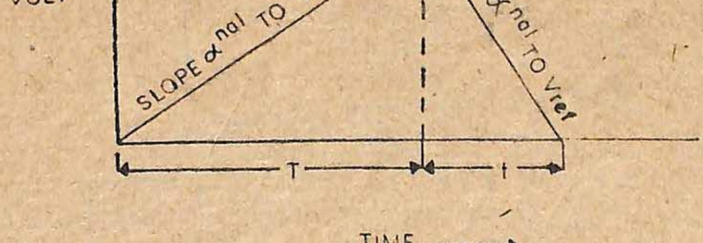


Fig. 63.1 (b)

conversion is made by connecting the integrator input to the unknown voltage through a switch for a known period of time *T*. This period of time is generated from an internal clock. During this period of the time, the integrator is switched on through an electronic switch which is usually a FET. During this period the capacitor gets charged up proportional to the input. When the input is high it is suitably attenuated so as not to saturate the integrator. During the second period of time *t* the capacitor is discharged through a constant reference voltage. This voltage, positive or negative is selected depending upon the nature of the input voltage. If the input voltage is positive the integration slope is negative and vice-versa. The discharge takes at a constant rate for an unknown period of time till the charged-up voltage across the integrator capacitor is brought to zero level. This unknown period of time is determined by counting clock pulses until the voltage across the capacitor reaches its basic reference level, (say, ground level in this example). The equation of voltage verses time can be written as

$$V_{in}/T_{fixed} = V_{ref}/t.$$

$$t = (V_{ref}/V_{in})\,T$$

where *T* is the fixed integration time. V_{in} is the unknown voltage.

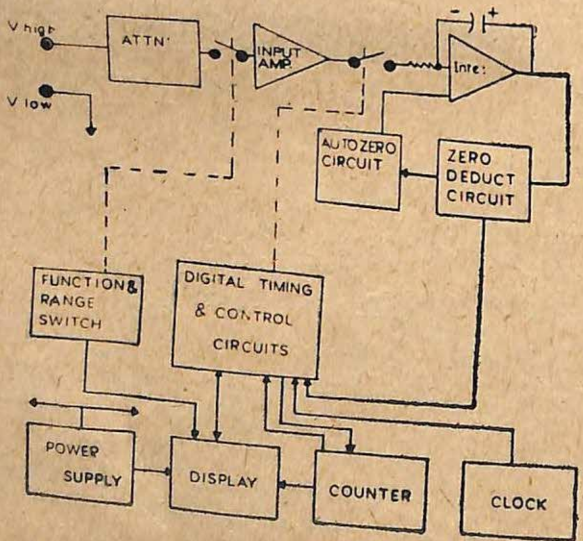


Fig. 63.2

V_{ref} is the reference voltage and t is the variable discharge time. This variable discharge time is digitised and fed through the counting circuit as in the frequency counter. The display of this is shown as voltage.

Modification on this basic voltmeter can be done to measure AC volt, current, and resistances. Since the basic function is that of measuring a DC voltage, AC is rectified using a rectifier circuit before feeding to the basic integrator. When the current is to be measured suitable shunts and precision series resistances are added to convert the current into proportional voltage. For ohms conversion a constant current source is actuated to get a voltage drop across the unknown resistance before feeding to the integrator circuit. A block diagram of a complete DVM is given in Fig. 63.2.

64

POWER SUPPLY

Most electronic devices and circuits require DC voltage to operate. In a laboratory d-c source can be generated from the AC mains using a power supply. Different circuits require varying degrees of levels of sophistication in the requirements of power. Some circuits require stringent ripple specifications and some other circuits require very strict regulations. All these can be combined in a single power supply which is available commercially. A series regulated power supply with provision for varying the voltage and current limitations is the best choice in a modern electronic laboratory.

A series regulated power supply is broadly illustrated in the block diagram shown in Fig. 64.1. The AC transformer suitably

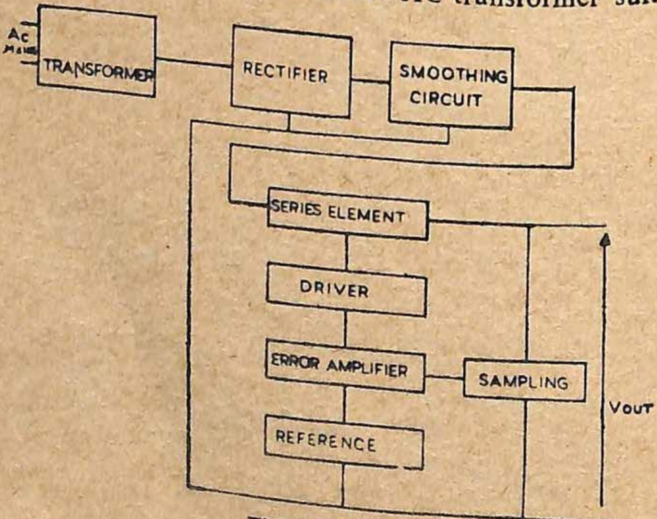


Fig. 64.1

steps down the voltage to the required designed value and the rectifier circuit converts this into DC voltage. The smoothing circuit reduces the ripple content to a great extent. This output is fed to a series regulator which regulates the voltage. In order to assist the series regulator to function, auxiliary circuits are required. The series regulator is driven by the Darlington combination known as the driver. The driver in turn is controlled by the error detecting amplifier. The amplifier has a ready reference voltage and a sampling of the output to enable it to detect the error and rectify it to have perfect regulation. A power supply having a capacity of 0-30 V, 1A will have the following desideration and components.

Transformer

From the AC mains of 230 V, 50 Hz the voltage is stepped down to about 32V rms, capable of giving a current slightly in excess of 1 amp. This transformer may have in addition to this main secondary, some other tappings also to enable amplifier and allied circuits to function in consonance with the main voltage.

Rectifier

The secondary voltages are rectified using appropriate range of rectifiers connected in the bridge configuration or centre tapped full wave configuration.

Smoothing Circuit

The rectified output will contain lot of AC elements. Depending upon the current rating and the smoothness required a simple capacitance smoothing circuit, capacitance and resistance smoothing circuit or capacitance and choke smoothing circuit is selected.

Series Element

Series element is a very important element in the chain of power supply circuit. This element handles entire power. A suitable rating for this element is a very essential factor. Good silicon transistors are now available in the market and the same can be used with suitable heat sinks. For example the maximum power which the series element has to dissipate is equal to $(V_{input}-V_{output})\times I_{output}$. V_{input} being constant, then power dissipation tends to increase with the reduction in V_{output} for a constant load. Generally 2*N* 3055 transistor with good heat sink is sufficient to handle the power for the power supply of the rating shown in the example.

Driver Circuit

The power transistor base requires some drive depending upon the output (load) current. This current will be all times less than load current. A transistor connected in Darlington combination will give the necessary drive.

Error Amplifier, Sample and Resonance Circuits

There is an amplifier to correct the output voltage. Initially the amplifier works with respect to a reference voltage and sample voltage fed to the emitter and to the base respectlively. When there is a variation in the output due to any reason the sample voltage changes. This causes a change in the base-emitter voltage. This in turn causes a change in the collector voltage which is passed on to the series element through the driver circuit. This will in turn rectify the defect in the output and tends to restore the actual voltage.

Power supplies are generally provided with short circuit and overload protection circuit. This enables the protection of the power supply against overloading and short circuiting for short durations. When power supplies are required to be used to energise loads at remote points, remote sensing terminals have to be used.

APPENDIX—A

I. *Diodes*

Type No.	PIV volts	I_F	I_O	P_T	T_J °C	$V_{F(max)}$ volts
BY 127	1250	1.2A	1.2A	5W	200	0.6
CD 31	20	50ma	50ma	150mw	150	0.8

PIV = Peak inverse voltage.
I_F = Forward DC current.
I_O = Average rectified current.
P_T = Power dissipation.
T_J = Junction temperature.
V_F = Forward voltage drop.

II. *Zener Diodes*

Type No.	V_Z	I_{ZM}	P_Z	T_J
CZ 5	2	25	200	150
CZ 6.2	6.2	25	200	150
CZ 12	12	25	200	150

V_Z = Normal zener voltage (Volts).
I_{ZM} = Maximum zener current (ma).
P_Z = Zener dissipation at 25°C ambient (mw)
T_J = Maximum junction temperature (°C)

III. *Tunnel Diode 1N3712*

Peak current $I_P = 5$ma.

Ratio of the peak current to the valley current $\frac{I_P}{I_V} = 5$.

Forward voltage peak point $V_P = 65$ mv.

Total capacitance (Junction capacitance) $C_J = 10$ pico farads.

Resistive cut off frequency $f = 2.3$ GHz.

Silicon Controlled Rectifier SN 101

Forward voltage drop at $I_F = 1$ Amp, $V_F = 1.5$ volts.
Reverse blocking current at PIV, $I_{r_1} = 100$ micro amperes.
Reverse blocking current at PIV, $T_A = 85°$ C, $I_{r_2} = 1$ ma.
Holding current $I_H = 10$ ma.
Gate trigger current $I_{GT} = 1$ ma (typical).
Reverse gate voltage $V_{GR} = 1$ volt.
PIV = 100 volts.

APPENDIX—B

I. *Transistors*

Type No.	V_{CBO}	V_{CEO}	V_{EBO}	I_C	P_T	L_J	f_T	I_{CBO}	h_{FE}
CIL231	−40	−40	−5	− 30	200	150	60	−0.5	50
CIL531	+40	+40	+5	+100	200	125	100	+0.5	40
CIL532	+40	+40	+5	+100	200	125	100	+0.5	100
CIL769	+40	+15	+4.5	+ 50	200	150	500	+0.4	40
2N464	−45	−40	−12	−100	600	85	1	−15	26
2N697	+60	——	+5	+800	600	175	1	+1.0	70
2N2369	+40	+15	+4.5	+500 (peak)	360	200	500	+0.4	40
2N3055	+100	+70	+1.8	+15000	115×10^3	200	0.8	——	30
AD149	−50	−30	−1.2	−3500	32.5×10^3	100	0.5	——	85

V_{CBO} = Collector—base voltage (volts).

V_{CEO} = Collector—emitter voltage (volts).

V_{EBO} = Emitter—base voltage (volts).

$I_{C(average)}$ = Collector current (ma).

P_T = Power dissipation at 25°C ambient (mw).

T_J = Junction temperature (°C).

f_T = Transition frequency (MHz).

$I_{CBO(max)}$ = Collector leakage current (micro ampere).

$h_{FE(min)}$ = DC current gain.

II. Unijunction Transistor 2N2647

Power dissipation $P_D = 300$ mw.
Interbase resistance $R_{BB(\min)} = 4.7$ kilo ohms.
Intrinsic standoff ratio $\eta = 0.68$.
Minimum valley current $I_{V(min)} = 8$ ma.
Maximum peak point current $I_{P(max)} = 2$ micro amperes.
Emitter saturation voltage at $I_E = 50$ ma, $V_{BB} = 10$ volts,
$V_{EB1(sat)} = 2$ volts.

III. Field Effect Transistor BEW10

Drain-source voltage $V_{DS} = 30$ volts.
Drain current $I_D = 20$ ma.
Power dissipation $P_D = 300$ mw.
Junction temperature $T_J = 200°C$.

APPENDIX—C

Integrated Circuit

1. *Operational Amplifier 741C*

Supply voltage = ±18 volts.
Differential input (max) = ±13 volts.
Operating temperature = 0 to 70°C.
Output voltage swing (max) = ±13 volts.
Output short circuit current = 25 ma.
Common mode rejection ratio = 20 db.
Slew rate = 0.5 volt/micro second.
Power consumption = 45 mw.

2. *Voltage regulator LM 723*

Pulse voltage from +V to −V (50 Msec)	50 volts.
Continuous voltage from +V to −V	40 volts.
Input/Output voltage differential	40 volts.
Differential input voltage	±5 volts.
Voltage between non-inverting input and −V	±8 volts.
Current from V_2	0.25 ma.
Current from V^2_{REF}	15 ma.
Internal power dissipation (metal can)	800 ma.
Storage temperature.	−65°C to 150°C.
Operating temperature range (723 C)	0°C to 70°C
Line regulation (typical)	0.01% of V_{out}.
Load regulation (typical)	0.02% of V_{out}.
Ripple rejection for frequencies from 50Hz to 10 kHz	74 db.
Average temperature coefficient of output voltage	0.002%/°C.
Input voltage range	40 volts.
Output voltage range	37 volts.

3. *Comparator LM 311*

Total supply voltage	36 volts.
Output to negative supply voltage	40 volts.
Ground to negative supply voltage	30 volts.

Differential input voltage	+30 volts.
Operating temperature	0°C to 70°C

	Typical	*Maximum*	*Unit*
Input offset voltage	2.0	7.5	mv.
Input offset current	6.0	5.0	na.
Input bias current	100.0	250	na.
Voltage gain	200	——	V/ma.
Response time	200	——	ns.
Input offset voltage	——	10	mv.
Input offset current	——	70	na.
Saturation voltage	0.23	0.40	V
Positive supply current	5.1	7.5	ma.
Negative supply current	4.1	5.0	ma.

4. *Timer LM 555*

Supply voltage	+18 volts max
Power dissipation	600 mw.
Operating temperature	0°C to 70°C.
Drift with temperature	50 ppm/°C.
Threshold voltage	$0.667\times V_{cc}$ typical
Trigger voltage for $V_{cc}=5$,	1.67 volts typical.
Reset voltage	0.7 volts typical
Rise time of output	100 ns.
Fall time of output	100 ns.

5. *NAND Gate SN 7400*

Input	*Output*
1-2	3
4-5	6
7 ground	
10-9	8
12-12	,,
$14+V_{cc}$	

Pin connections

Input	*Output*
1,2	3
4,5	6
9,10	8
12,13	11

Pin 14 is connected to power supply positive and 7 is connected to power supply negative and ground.

Supply voltage	5 volts typical.
High level output current	−400 micro amperes

Low level output current	0.16 ma.
Operating temperature	0°C to 70°C
V_{iH} High Level input voltage	2 Volts minimum.
V_{iL} Low level input voltage	0.8 maximum.
V_{oH} High level output voltage	2.4 minimum, 3.4 volts typical
V_{oL} Low level output voltage	0.2 typical, 0.4 maximum.
I_1 Input current at maximum input voltage	1 ma. max.
II_{iH} High level input current	40 micro amp. max.
III_{iL} Low level input current	−1.6 ma. max.

REFERENCES

ALFRED GRONER, "Outline of Transistor Circuit Analysis" (Regents Publishing Company, Inc., New York, 1966).

BRINTON B. MITCHELL, "Semiconductor Pulse Circuits with Experiments" (Holt, Rinehart and Winston Inc., New York, 1970).

CHARLES L. ALLEY AND KENNTH ATWOOD, "Semiconductor Devices and Circuits" (John Wiley and Sons Inc., New York).

DWARKANATA, T., "Guide to Practicals in Electronics" (Asia Publishing Co., Bombay, 1969).

FRANKLIN C. FITCHEN, "Transistor Circuit Analysis and Design" (D. Van Nostrand Company, Inc., New York, 1968).

HIMANSHA, B. DAVE, "Laboratory Experiments in Digital Systems" (The Macmillan Co. of India Ltd., Delhi, 1977).

JOHN DOUGLAS—YOUNG, "Complete Guide to Electronic Test Equipment and Trouble Shooting Techniques" (Parker Publishing Company, Inc., New York, 1975).

RAMABADRAN, S., "Electronics, Principles and Techniques" (S. Chand & Co. Ltd., New Delhi, 1976).

RICHARD F. SHEA, "Transistor Circuit Engineering" (John Wiley and Sons, Inc., New York, 1959).

ROBERT F. COUGHLIN, "Solid State Devices and Applications" (Prentice Hall, Inc. New Jersey, 1975).

SOL D. PRENSKY, "Electronic Instrumentation" (Prentice Hall, Inc., New Jersey, 1971).

SONI, M.L., GUPTA, I.C. and GUPTA, P.V., "A Course in Electrical Circuits and Fields" (Dhanpur Rai & Sons, Delhi, 1968).

A LABORATORY COURSE IN ELECTRONICS

T. RAMALINGOM & P. RAGHUPALAN

The use of inductive reasoning and experimentation provide the most important means of understanding nature. Experimentation not only helps in verification but also in gaining new insights. The basic tool, therefore, in engineering practice, besides mathematical analysis and engineering judgement is laboratory or field experiments. Laboratory institution must aim at training and educating a student, in utilising the experimental method for solving problems.

A Laboratory Course in Electronics is a very valuable contribution as there are not many good books on Laboratory practice.

The book gives a comprehensive laboratory course. It contains 54 kinds of carefully chosen circuits of high practical and professional importance. Besides giving a procedure for conducting experiments, some insight into the basic principles and design consideration is given to coordinate practical approach and theory.

A separate part covers various kinds of test and measuring equipment used in a laboratory.

This book should satisfy the need of engineering colleges, polytechnics and other technical institutions which are offering courses in electronics and electrical engineering.

PRICE
Rs 39-00 00

OXFORD & IBH PUBLISHING CO.
New Delhi Bombay Calcutta

ISBN 81-204-0057-7